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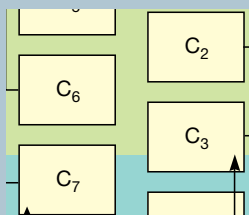
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PQFN (5x6)			
Part	V	nC	mΩ
IRFH5303	30	15	4.2
IRFH5304	30	16	4.5
IRFH5306	30	7.8	8.1
IRFH5301	30	37	1.9
IRFH5302	30	4.8	2.1
IRFH5302D	30	26	2.5

PQFN (3x3)			
Part	V	nC	mΩ
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IRFHM830D	30	13	4.3

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BY PATRICK MANNION, DIRECTOR OF CONTENT

## Finding the best part just got easier

**A**s you know, *EDN* is all about connecting you with your peers, inspiring you with their successes, and helping you to get your design done—on time, to spec, and within budget—with as few sleepless nights and long weekends as possible. We accomplish this goal in many ways. In print, we provide straightforward engineer-to-engineer technical features and regular columns from industry insiders, as well as product and trend features and write-ups from our engineer-editors, all of whom have spent at least some of their career dealing with the issues you face every day. Online, the world opens wide with webinars, courses, webcasts, and real-time commentary and dialogue among writers, contributors, and readers.

That interaction is all well and good; for engineers, however, all the studying, coursework, webcasts, and peer-to-peer discussion may help you home in on the part you need, but it won't help you find the right part at the right time from the right vendor. And the right part, as you know, can make or break a design.

Anyone who's been tracking the business of providing product information and data knows that companies have risen, striven, and died based on the belief that they could help you make that device or component selection easier than anyone else, and some have prevailed. With that idea in mind, I'm excited to guide you to our latest service, [www.datasheets.com](http://www.datasheets.com), and what I think is the best free site out there to help you find, select, and obtain the part you need when you need it.

The result of a partnership between *EDN*'s owner, UBM Electronics, and SiliconExpert Technologies, [Datasheets.com](http://www.datasheets.com) hosts data sheets and information on 185 million parts—and growing—and is rife with selection features, including parametric searches, saved searches, parts comparisons, and inventory watches. Independent com-

panies have in the past provided parametric-search capabilities for specific parts—microcontrollers, for example—but this task is difficult to do for everything from resistors to power devices and processors. [Datasheets.com](http://www.datasheets.com) does it and does it well. It also allows you to save your searches and go back to them later.

[Datasheets.com](http://www.datasheets.com)'s parts-comparison feature lets you compare as many as four parts side by side, although I recommend doing only two at once because comparing four can get unwieldy. And the inventory-watch feature alerts you when your favorite distributor gets the necessary amount in stock of a part you want. The site also includes product announcements; when you register, you automatically get a regular e-mail alert on the latest new products.

SiliconExpert faced difficulties in assembling a useful parts-search database. According to Vineet Chaudhary, product-marketing manager at the company, the challenge is twofold: getting as much of the right data as possible and then “normalizing” it to make it useful.

“Some sites just crawl the Web and grab data sheets, and you can't navigate

them,” says Chaudhary. “All they want is to get as many as possible and get indexed on Google.”

SiliconExpert instead focuses on building solid relationships with both manufacturers and distributors to ensure a steady feed into the database of all their products. This approach gets perhaps 80% of the available products. Some Web crawling is necessary to find smaller companies' products and close the gap to get as close to 100% of available products as possible.

However, getting the data is only half the battle. The real work starts with normalizing it. As all engineers are aware, some specsmanship is always at play, and manufacturers may emphasize particular specs over others or omit a spec altogether.

**Getting the data is only half the battle. The real work starts with normalizing it.**

“You have to read between the lines,” says Chaudhary. “There's no ‘standard’ to compare, so it makes it hard for engineers; that's where we come in.”

SiliconExpert has 250 engineers working on making data sheets from myriad vendors comparable. And these are real engineers, Chaudhary adds, making the point that much of the intellectual property resides in the algorithms used to normalize the data. The engineers are constantly working to optimize these algorithms.

Although SiliconExpert has been performing these services since 2000, the company is constantly changing. “[Electronics is] a mature industry,” says Chaudhary, “but with software we can always add new features.” One feature in the works is a customized alert to engineers for new-product introductions.

What do you think? After all, it's your tool, so I'd love to hear what you think and how we can enhance it. I look forward to your feedback.**EDN**

Contact me at [patrick.mannion@ubm.com](mailto:patrick.mannion@ubm.com).

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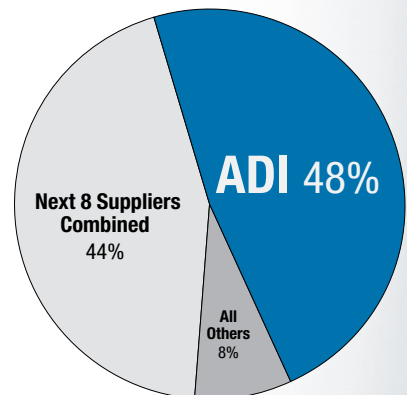


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# pulse

INNOVATIONS & INNOVATORS

## 33-GHz, 100G-sample/sec scope claims industry's best accuracy

**T**ektronix has announced the DPO (digital-phosphor oscilloscope)/DSA (digital-signal analyzer) 70000D series, which comprises four models. With two channels active, real-time acquisition rates range to 100G samples/sec on each channel, and, depending on the model, analog bandwidth reaches either 25 or 33 GHz. For repetitive—though not necessarily periodic—signals, you can use the random-equivalent-time-sampling feature to obtain 25- or 33-GHz bandwidth on four channels with effective acquisition rates on each channel as high as 10,000G samples/sec. With real-time sampling, the bandwidth on each of the four channels is 20 GHz, although the manufacturer believes that it will upgrade this specification to 22.5 GHz once the evaluation of production quantities is complete.

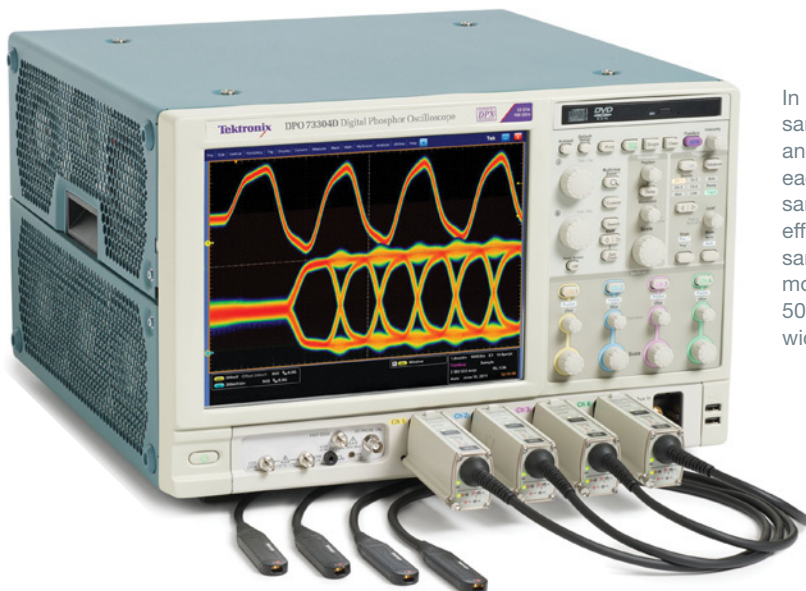
According to Tektronix, these instruments provide the highest available measurement accuracy for today's fastest multichannel electrical signals. Analysis of optical modulators and characterization of SERDES (serializer/deserializer) devices require accurate measurements at bit rates beyond 20 Gbps. Such measurements require test instruments that deliver low noise and high sensitivity. Using an IBM (www.ibm.com) SiGe (silicon-germanium)-fabrication process, Tektronix engineers have produced ICs that integrate high-speed bipolar transistors and standard CMOS on one die, enabling the new instruments to deliver low noise and the fastest multichannel rise time of any real-time scopes, according to the company. US suggested list prices start at \$202,000. —by Dan Strassberg

► Tektronix Inc, www.tektronix.com.

### TALKBACK

**"The competitive demands to be 'best in class' can optionally be addressed by even more thorough testing to even tighter performance limits. This [article's] analysis will remain completely appropriate until someone learns how to wave a magic high-precision wand over each warm wafer."**

—Analog Devices fellow  
Barrie Gilbert, in EDN's Talkback section, at <http://bit.ly/oj1t1O>.  
Add your comments.



In real-time mode, the DPO73304D takes 100G samples/sec on two channels simultaneously and delivers bandwidth as great as 33 GHz on each channel. By using random-equivalent-time sampling on repetitive signals, the scope can, in effect, sample 100 times as fast and obtain the same bandwidth on four channels. In real-time mode on four channels, the acquisition rate is 50G samples/sec on each channel, and bandwidth is 20 GHz.

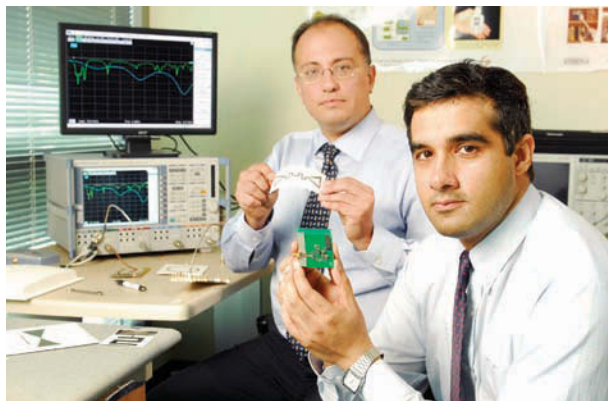
## Researchers harvest ambient electromagnetic energy as power source

Researchers at the Georgia Institute of Technology have found a way to capture and harness ambient energy from such sources as radio and television transmitters, cell-phone networks, and satellite-communications systems. They believe that the technique could provide a new way to power networks of wireless sensors, microprocessors, and communications chips.

"There is a large amount of electromagnetic energy all around us, but nobody has been able to tap into it," says Manos Tentzeris, a professor in the school of electrical and computer engineering who is leading the research. "We are using an ultrawideband antenna that lets us exploit a variety of signals in different frequency ranges, giving us greatly increased power-gathering capability."

According to the university, the team's scavenging devices can convert energy from communications devices from ac to dc and store it in capacitors and batteries. The scavenging technology currently can take advantage of frequencies from FM radio to radar, a range spanning 100 MHz to 15 GHz or higher.

Scavenging experiments using TV bands have yielded power amounting to hundreds of microwatts, and multiband



Georgia Tech graduate student Rushi Vyas (front) holds a prototype energy-scavenging device, and Professor Manos Tentzeris displays a miniaturized flexible antenna that could find use in broadband-energy scavenging.

systems should generate 1 mW or more—enough to operate many small electronic devices, including a variety of sensors and microprocessors, the school reports. The researchers expect that, by combining energy-scavenging technology with super-capacitors and cycled operation, the technology can power devices requiring more than 50 mW. In this approach, energy builds up in a battery-like super-capacitor that the device uses when the capacitor reaches the required power level.

The researchers have successfully operated a temperature sensor using electromagnetic energy they captured from a television station 0.5 km away. They are preparing another dem-

onstration in which they will activate a microprocessor-based microcontroller simply by holding it in the air. Tentzeris notes that exploiting a range of electromagnetic bands increases the dependability of energy-scavenging devices because the system can exploit other frequencies if one frequency range temporarily fades due to usage variations.

The researchers further note that the scavenging device could work alone or in tandem with other generating technologies or could provide system backup. For example, if a battery or a solar-collector/battery package failed completely, scavenged energy could allow the system to transmit a wireless distress signal and still

maintain critical functions.

The researchers are using ink-jet printers with silver nanoparticles or other nanoparticles in an emulsion to combine sensors, antennas, and energy-scavenging capabilities on paper or flexible polymers. This approach allows the team to print not only RF components and circuits but also novel sensing devices employing nanomaterials such as carbon nanotubes.

When Tentzeris and his research group began ink-jet printing of antennas in 2006, the paper-based circuits functioned at frequencies of only 100 or 200 MHz, recalls Rushi Vyas, a Georgia Tech graduate student working on the project. "We can now print circuits that are capable of functioning at up to 15 GHz—60 GHz if we print on a polymer," Vyas says. "So we have seen a frequency-operation improvement of two orders of magnitude."

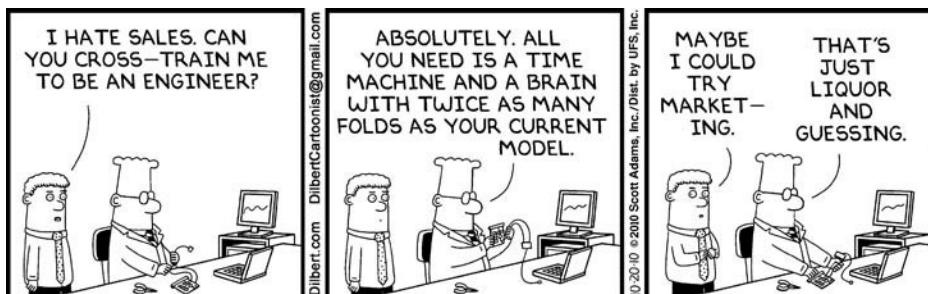
The resulting self-powered wireless sensors could find use in chemical, biological, heat, and stress sensing for defense and industry; RFID (radio-frequency-identification) tagging for manufacturing and shipping; and monitoring tasks in communications and power usage. The researchers believe that these self-powered, wireless, paper-based sensors will soon be widely available at low cost.

The researchers gave a presentation on the technology last month at the IEEE Antennas and Propagation Symposium in Spokane, WA. Sponsors of the research include the National Science Foundation ([www.fhwa.dot.gov](http://www.fhwa.dot.gov)), the Federal Highway Administration ([www.fha.org](http://www.fha.org)), and Japan's New Energy and Industrial Technology Development Organization ([www.nedo.go.jp/english/index.html](http://www.nedo.go.jp/english/index.html)).

—by Suzanne Deffree

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### DILBERT By Scott Adams







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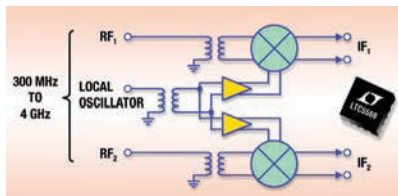
CHANGING THE STANDARDS



## Dual broadband RF mixer finds use in 4G base-station receivers

Linear Technology has introduced the dual, high-performance LTC5569 RF mixer, which operates at 300-MHz to 4-GHz frequencies. The highly linear part has an input IP3 (third-order intercept) of 26.8 dBm, an output IP3 of 28.8 dBm, and a conversion gain of 2 dB. The IC has a noise figure of 11.7 dB, or 17 dB with a 5-dBm inband blocking-interference signal. The LTC5569 operates from a single 3.3V supply, and power consumption is 600 mW when you enable both mixers. When you disable the mixers, the IC has a maximum 200- $\mu$ A leakage current. You can independently shut down either channel using a separate enable control. Turning on and off the channels does not induce a load disturbance, which might unlock the PLL (phase-locked-loop) and VCO (voltage-controlled-oscillator) circuits.

Each channel of the LTC5569 dual mixer contains an on-die integrated balun (balanced-unbalanced) transformer at the RF and local-oscillator inputs. These single-



The LTC5569 dual broadband mixer has on-die balun transformers.

ended ports are matched at 50 $\Omega$ . Each channel's local oscillator has separate buffers you drive from a common input, providing channel-to-channel isolation and preserving phase coherency between the two channels. The

local oscillator's input port is always matched at 50 $\Omega$ , regardless of whether the mixer is on or off. The local oscillator's input requires a 0-dBm drive level, and it has excellent reverse-RF isolation. You can drive it directly from an external VCO circuit.

The IC targets use in the new generation of multiple receivers in 4G (fourth-generation) base stations. It eases the thermal design challenge in MIMO (multiple-input/multiple-output) remote-radio-head designs, which pack as many as 16 channels of receivers into small, weather-sealed housings. You can configure the part to operate on 700-MHz to 2.7-GHz cellular bands.

Linear Technology specifies the LTC5569 for a case operating temperature of -40 to +105°C and offers it in a 4x4-mm QFN package. It costs \$8.50 each (1000). Samples and production quantities are available.

—by Paul Rako

► **Linear Technology,**  
www.linear.com/product/LTC5569.

## VNAs add dynamic range, cut measurement times

Targeting use in the production and development of RF components, the ZNB and ZNC VNAs (vector network analyzers) from Rohde & Schwarz feature a dynamic range as high as 140 dB and a sweep time as low as 4 msec for 401 points. Both the ZNB and the ZNC have a 12.1-in.-diagonal touchscreen that allows users to access all instrument functions with no more than three operating steps.



The ZNB and ZNC VNAs feature a dynamic range as high as 140 dB and a sweep time as low as 4 msec for 401 points.

The ZNB, the more powerful of the two instruments, provides development labs and production lines with performance characteristics previously found only in high-end analyzers. The ZNB covers the

frequency range of 9 kHz to 4.5 GHz or 8.5 GHz and is available in both two- and four-port models. It features a dynamic range of 140 dB, trace noise of 0.004 dB rms, and output power as high as 13 dBm, which users can adjust electronically over a 90-dB range. The ZNB's low magnitude and phase drift result in temperature and long-term stability to minimize the need for recalibration. The ZNB suits use in the measurement of high-blocking filters or amplifiers that operators must manually adjust on high-volume production lines in which speed and efficiency are critical. You can also use the network analyzer to characterize duplex filters, multiport DUTs (devices under test), mixers, or differential SAW (surface-acoustic-wave) filters for transmitters or mobile terminals.

The ZNC, with a frequency range from 9 kHz to 3 GHz, is an alternative for users who have lower requirements regarding dynamic range and functional scope. The ZNC is available with two test ports and offers a sweep time of 11 msec with 401 points and a dynamic range as high as 130 dB. Its primary use is for testing passive RF components, such as filters and cables.

The touchscreen on both instruments eliminates the need for using submenus or nested menus. With the ZNB and the ZNC, all context-based control elements are directly available on the soft panel, and all instrument functions are accessible in three or fewer operating steps. Simply by touching the screen, users can create measurement windows, shift traces, set markers, adjust scales, and zoom in and out for detailed analyses. Users can arrange and instantaneously call up instrument setups on individual tabs, allowing the efficient characterization of DUTs such as amplifiers or RF modules. The user interface and online help are available in English, Chinese, Japanese, French, and Russian.

Measuring 18.2x9.6x13.9 in., the ZNB and ZNC leave room on the workbench measurement. Test cables' small bending radii can sometimes cause problems, and the units' widely spaced test ports below the touchscreen eliminate these issues, resulting in fewer phase errors and less cable wear. Low power consumption and sophisticated cooling minimize operating noise and heat dissipation and reduce operating costs. —by Rick Nelson

► **Rohde & Schwarz,**  
www.rohde-schwarz.com/product/znb and www.rohde-schwarz.com/product/znc.

# Scope software frees probe de-embedding from tedious calibration

**A**gilent Technologies has announced the N2809A PrecisionProbe software package for its Infiniium 90000X and 90000A series oscilloscopes. The software, which works with the scopes' built-in hardware, automatically and without using external equipment characterizes and corrects the response of any signal path to a scope input. The software's analyses increase measurement margins, which probe setups can reduce without warning that they have done so.

Although the design of advanced probing systems, such as Agilent's Infiniimax III, minimizes losses, cables and probes are inherently lossy. Depending on the configuration, the loss can sometimes be substantial. At other times, the loss can be just enough

to cause measurement variations that produce inconsistent results. Moreover, frequency response and phase characteristics can vary from probe to probe, so you must characterize and account for each probe and cable to ensure that



PrecisionProbe software teams up with built-in hardware in the manufacturer's top-of-the-line scopes to improve the accuracy of scope-based measurements and remove the tedium and errors that often accompany calibration of probes, cables, fixtures, and such accessories as signal switches.

the scope provides the truest possible representation of the signal. The N2809A software helps you to overcome these challenges by quickly correcting for cable and channel insertion loss; correcting probing issues, such as phase nonlinearity and lack of magnitude flatness; matching both the frequency and phase response of every cable and probe in your setup; characterizing and compensating for loss in channel paths, such as switches, without adding equipment; and characterizing probe-impedance profiles.

According to Agilent, PrecisionProbe is the first software on real-time oscilloscopes to provide full ac-probe calibration—not just dc calibration or skew correction. PrecisionProbe does not depend on externally generated S-parameter-characterization files. Creation of these files, which commonly requires the use of such additional instruments as time-domain reflectometers or vector network analyzers, can be time-consuming and requires considerable operator expertise to produce accurate and consistent results. Instead, PrecisionProbe uses a signal source in the scope to automatically generate the files. The software's setup wizard quickly moves you through setting up and characterizing such channel elements as probes, cables, and switches. Prices start at \$5000. —by **Dan Strassberg**  
▶ **Agilent Technologies**, [www.agilent.com/find/PrecisionProbe](http://www.agilent.com/find/PrecisionProbe).

## Automotive platform offers advanced debugging and security

**Green Hills Software** recently enhanced its automotive platform, adding a processor-trace-probe update, improved compiler performance and footprint, and native support for the company's Integrity real-time OS targeting Freescale's ([www.freescale.com](http://www.freescale.com)) Qorivva automotive microcontrollers. The announcement reinforces Green Hills' commitment to the automotive market, following its recently joining the Genivi Alliance ([www.genivi.org](http://www.genivi.org)), a nonprofit alliance pushing the broad adoption of an in-vehicle-infotainment reference platform.

The trace-probe enhancement targets applications such as ECUs (electronic-control units), with many specialized processing elements that must meet the demands of OEMs and their tier-one suppliers. In these cases, trace capability tracks bugs with faster processors, translating to a requirement for more memory to record execution histories. To address this concern, Green Hills has upgraded its nonintrusive SuperTrace Probe Version 3 with 4 Gbytes of trace-memory collection through IEEE's Nexus Class 3 interface, with an option to upgrade to 8 Gbytes. The previous limit was 1

Gbyte. With the company's TimeMachine back-in-time debugger, users can now more easily trace bugs that they previously may have overlooked. The new trace adapter also supports 5V interfaces.

For performance, Green Hills used optimizing compilers for EEMBC (Embedded Microprocessor Benchmark Consortium) Automark scores for Freescale's 32-bit Qorivva MPC5566, 5607B, 5644A, and 5674F microcontrollers. The results for the 5674F, according to Green Hills, rank as the highest for an automotive microcontroller.

For automotive security, Green Hills has ported its Integrity RTOS to the MPC5688G. The device's compilers can build the RTOS and applications with variable-length encoding, enabling a 20% code-size reduction. The company has added full support for variable-length-encoding debugging to Multi to support run-mode, stop-mode, and OS-aware debugging. The board-support package also supports SPI (serial-peripheral interface) and I<sup>2</sup>C (inter-integrated-circuit) and CAN (controller-area-network) interfaces. —by **Patrick Mannion**

▶ **Green Hills Software**, [www.ghs.com](http://www.ghs.com).

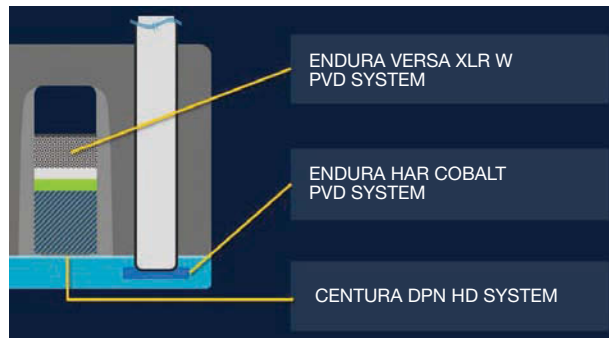
## Applied tunes up transistors for DRAM makers

Applied Materials recently introduced a series of chemistry and equipment changes. The move indicates the degree to which physics, chemistry, and the semiconductor-equipment industry must push ahead increasingly reluctant transistor performance in silicon-gate MOSFETs in the peripheral circuitry, including the address decoders, sense amps, and multiplexers, of advanced DRAMs. Unlike logic processes, which have converted to high-k/metal-gate MOSFETs at advanced nodes, DRAM processes have stayed with the significantly simpler silicon-gate stack. The array transistors in the memory cells have undergone an intense evolution, now employing recessed channels to get adequate performance at a tiny size. The peripheral transistors, however, have stayed about the same through succeeding generations to the point at which they have become the weak link in improving DRAM performance.

Applied Materials is aiming the equipment and chemistry announcements at three components in the peripheral transistor's equivalent circuit. The Versa XLR (extremely low-resistance) Tungsten PVD (physical-vapor-deposition) tool attacks gate-electrode resistance and parasitic capacitance. The DPN (decoupled-plasma-nitridation) HD (high-dose) tool increases k in the gate dielectric, allowing better switching speed and leakage control. And the HAR (high-aspect-ratio) Cobalt PVD tool works on contact resistance.

The Versa XLR, a modification of Applied's Versa PVD tool, produces large-grained, low-defectivity tungsten films exhibiting low resistivity. The tool cre-

ates the tungsten layer at the top of the gate stack, between the interconnect metal and the lower layers that end at the polysilicon-gate material. Because of the lower resistivity of the low-defec-



Applied is attacking transistor performance at the gate-electrode, gate-oxide, and contact areas.

tivity, large-grained film, process engineers can make the film significantly thinner—350 Angstroms instead of 450, Applied claims—which in turn reduces the sidewall capacitive coupling to adjacent gate structures.

The DPN HD tool is not a PVD chamber but a plasma reactor to drive nitrogen into the gate oxide. Process engineers

employ nitriding because, at approximately the 130-nm logic node, the approach improves gate capacitance. But there is an undesirable side effect: Higher nitrogen concentrations also lead to higher threshold voltages. Applied claims to have found a way around this trade-off, giving a combination

to a high-k gate dielectric and a metal-gate electrode.

The HAR Cobalt PVD system replaces titanium silicide with cobalt silicide at the interface layer at which the tungsten contact touches the source and drain silicon. The nature of DRAM processes means that the contact plugs for source and drain contacts have a high aspect ratio: Instead of the typically shallower than 1-to-3 trenches for logic processes, DRAM-peripheral-transistor contact holes are via holes with depths as much as seven times their diameters. In this environment, with decreasing geometries, what was once a smooth titanium film at the bottom of the hole has become a little clump somewhere at the bottom of the via, resulting in high and highly variable contact resistance.

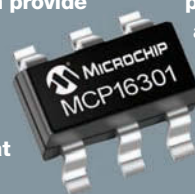
The company thus switched from titanium to vapor-deposited cobalt, which forms a smooth, conformal film over the bottom of the contact hole, allowing creation of a uniform silicide layer and improving both contact resistance and variability.

—by Ron Wilson

►Applied Materials,  
[www.appliedmaterials.com](http://www.appliedmaterials.com).

### 30V BUCK SWITCHING REGULATOR ACHIEVES 95% EFFICIENCY

**Microchip Technology's new 30V-input MCP16301 buck switching regulator features a 600-mA output and a 4 to 30V input-voltage range. The chip integrates a high-side switch and can output a voltage of 2 to 15V. It can provide as much as 95% efficiency. High-speed peak-current-mode control allows fast responses to sudden input-voltage and load transients that power applications frequently encounter. Integrated control-loop and slope compensation make it easy to reliably stabilize the converter-control system.**



The MCP16301 buck regulator can output 600 mA and provide efficiency as high as 95%.

**The IC targets use in the industrial, telecommunications, consumer, and automotive markets, such as set-top boxes, LED lighting, HVAC (heating/ventilation/air-conditioning) systems, and power meters. It uses less power and dissipates less heat than does a low-dropout regulator.**

**A D2PAK footprint demo board with 300-mA outputs is available for \$14.99, and a 600-mA demo board sells for \$19.99. The MCP16301 is available in a six-pin SOT-23 package and sells for 83 cents (10,000).**—by Paul Rako

►Microchip Technology,  
[www.microchip.com/get/TQEG](http://www.microchip.com/get/TQEG).

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# TEST 18-BIT ADCs WITH AN ULTRAPURE SINE-WAVE OSCILLATOR

WITH CAREFUL  
DESIGN,  
THIS CIRCUIT  
CHALLENGES TEST  
EQUIPMENT'S  
ABILITY TO  
VERIFY ITS  
PERFORMANCE.

BY JIM WILLIAMS AND GUY HOOVER • LINEAR TECHNOLOGY

**T**he ability to faithfully digitize a sine wave is a sensitive test of high-resolution-ADC fidelity. This test requires a sine-wave generator with residual distortion products approaching 1 ppm (part per million). It also requires a computer-based ADC-output monitor to read and display the converter's output spectral components. Performing this testing at reasonable cost and complexity requires the construction of its elements and performance verification before its use. A low-distortion oscillator drives the ADC through an amplifier (**Figure 1**). The ADC's output interface formats the converter output, which communicates with the computer. The computer executes spectral-analysis software and displays the resulting data.



IMAGE: ISTOCKPHOTO.COM

## OSCILLATOR CIRCUITRY

The system's oscillator is the most difficult-to-design part of the circuit. The oscillator must have transcendently low levels of impurity to meaningfully test 18-bit ADCs. You must then verify these impurity characteristics by independent means.

Start with a design based on the work of Winfield Hill, director of the electronics-engineering laboratory at the Rowland Institute at Harvard University. You can then adapt this design for a 2-kHz Wien-bridge design (Figure 2). Using all of the amplifiers in inverting mode eliminates CMRR (common-mode-rejection-ratio) errors from the signal path.

Low-distortion amplifiers  $A_1$  and  $A_2$  are the active components of this oscillator. The JFET of the original design would introduce conductivity-modulation errors, so you can replace it with an LED-driven CdS (cadmium-sulfide) photocell isolator. You then combine the output of  $A_2$  with a filtered dc offset at the input to  $A_3$ . The capacitor in  $A_3$ 's

### AT A GLANCE

Measuring 18-bit ADCs requires a good oscillator.

You can adapt a Wien-bridge circuit.

A photocell performs AGC (automatic gain control) better than does a JFET.

Be sure to verify the oscillator's circuit performance with calibrated test equipment.

feedback network limits the bandwidth of the amplifier. The output of this 2.6-kHz filter drives the input amplifier of the ADC under test.

The  $A_1/A_2$  oscillator needs AGC (automatic gain control), so you couple the circuit's output to a high-impedance, low-noise JFET-input amplifier,  $A_4$ , which feeds precision rectifier  $A_5$ .  $A_5$  in turn drives integrator  $A_6$ .  $A_6$ 's dc output represents the ac amplitude of the circuit's output sine wave.

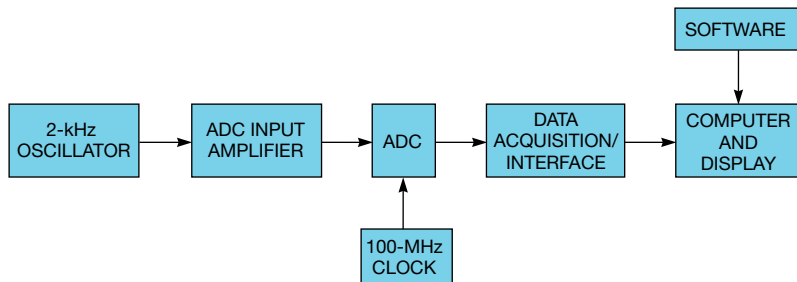


Figure 1 In a spectral-purity test system for an ADC and a distortion-free oscillator, the computer displays the Fourier components due to amplifier and ADC infidelity.

# Identifier.

## Active RFid reference design

- ▶ Real time location system (RTLS)
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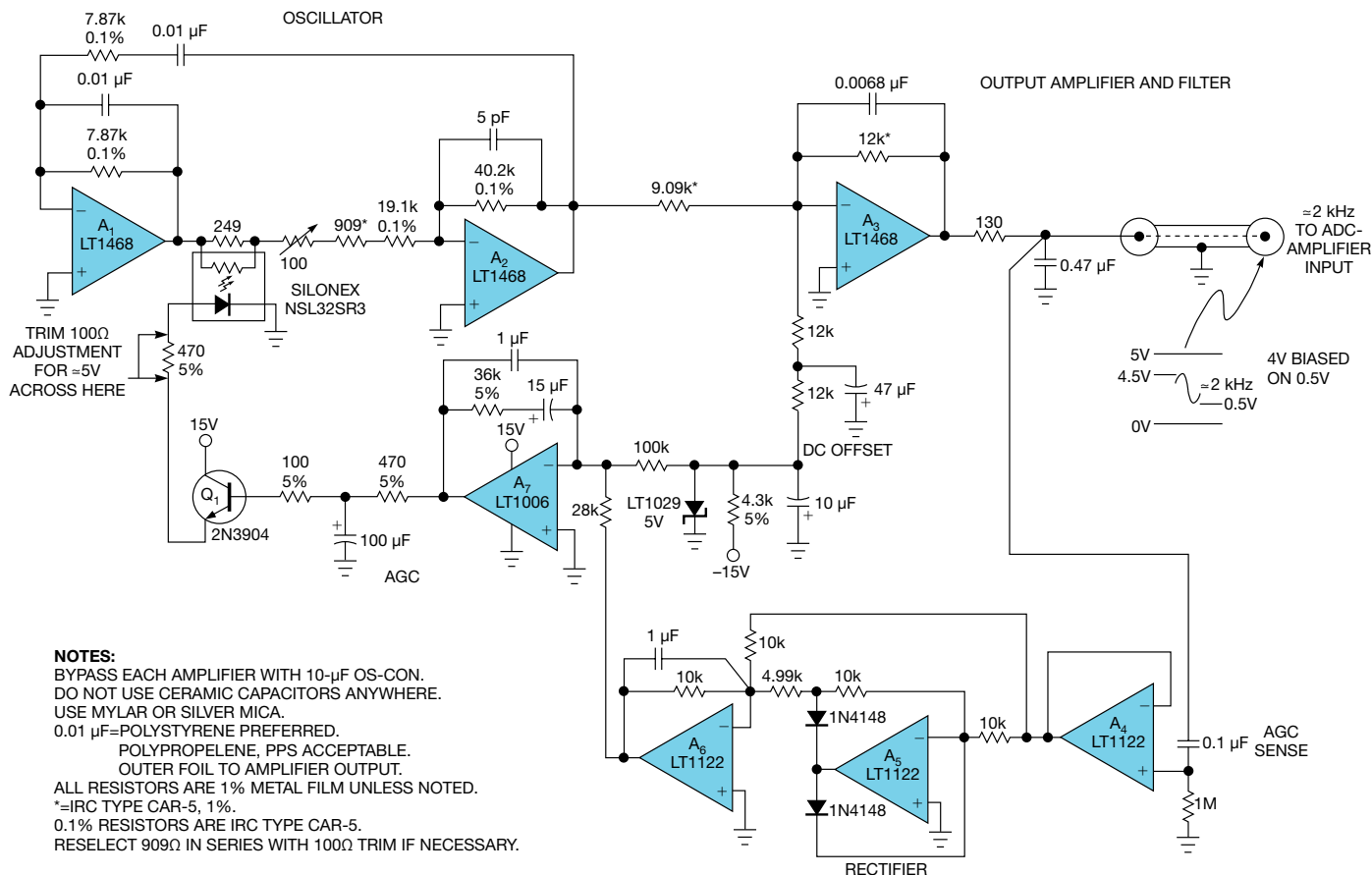


Figure 2 A Wien-bridge oscillator uses inverting amplifiers in the signal path and achieves 3-ppm distortion. An LED photocell replaces the usual JFET as gain control.

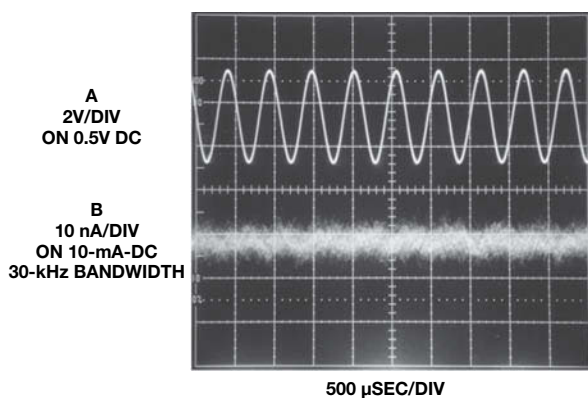


Figure 3 Trace A is the oscillator's output. Related residue (Trace B) is just discernible in  $Q_1$ 's emitter noise. At approximately 1 nA, it represents 0.1 ppm of LED-current variation. Heavy AGC signal-path filtering prevents modulation products from influencing the photocell response.

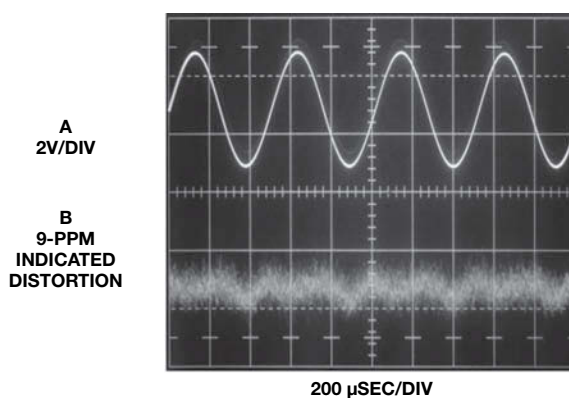


Figure 4 An HP-339A distortion analyzer operating beyond its resolution limit provides misleading distortion indication (Trace B). The analyzer output contains an unreliable combination of oscillator and instrument signatures. Trace A is the oscillator's output.

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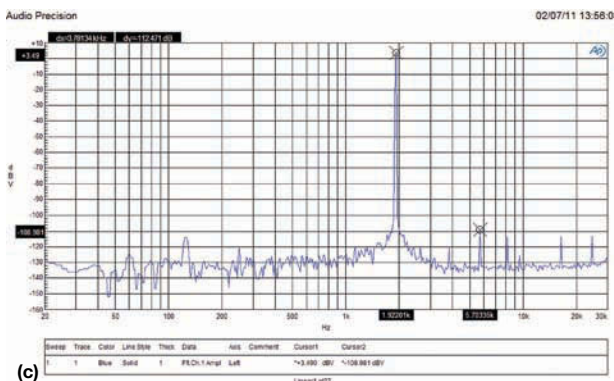
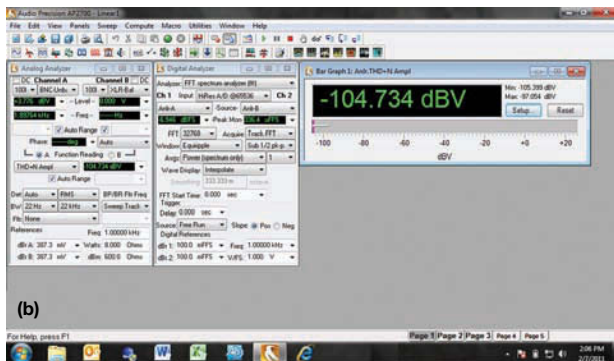
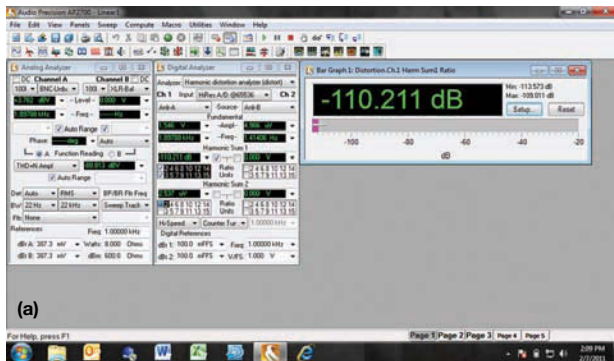
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**Figure 5** The Audio Precision 2722 analyzer measures oscillator THD at -110 dB, or approximately 3 ppm (a). The analyzer measures oscillator THD+N at -105 dB, or approximately 5.8 ppm (b). Its spectral output indicates a third harmonic peak at -112.5 dB, or 2.4 ppm (c).

Current-summing resistors can be used to balance the dc value against a voltage reference that the Linear Technology (www.linear.com) LT1029 IC creates. The current-summing resistors feed the AGC single-supply amplifier,  $A_7$ . This amplifier drives  $Q_1$ , which sets the LED current. The LED current closes a gain-control loop because it ultimately varies the CdS cell's resistance, stabilizing the oscillator's output amplitude.

By deriving the gain-control feedback from the circuit's output, you maintain the output amplitude, despite the attenuating, bandlimiting response of  $A_3$  and the output filter. This topology also places demands on the loop-closure dynamics of amplifier  $A_7$ ,  $A_3$ 's bandlimiting, the output filter,  $A_6$ 's lag, and the ripple-reduction components that attach to  $Q_1$ 's base com-

bine to generate a significant amount of phase delay. You can accommodate this delay with a 1- $\mu$ F dominant pole at  $A_7$ , along with a zero-value RC (resistor/capacitor), to achieve stable loop compensation. This approach replaces closely tuned high-order output filters with simple RC roll-off responses, minimizing distortion and maintaining constant output amplitude.

It is essential that you eliminate oscillator-related signal components from the LED bias to maintain low distortion. Any such residue modulates the oscillator's amplitude, introducing impure frequency components. The bandlimited AGC signal path is well-filtered.

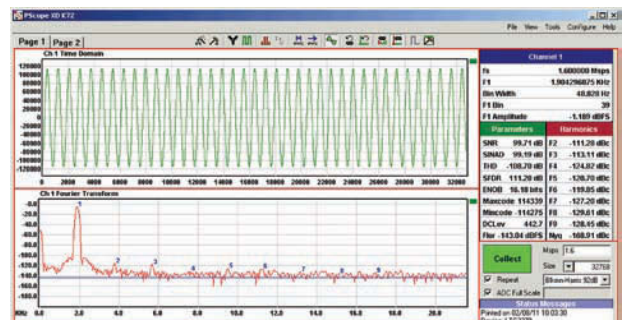
The heavy RC time constant in  $Q_1$ 's base provides a final, steep roll-off response.  $Q_1$ 's emitter current shows approximately 1 nA of oscillator-related ripple from a 10-mA total—less than 0.1 ppm (Figure 3). The oscillator needs only one 100 $\Omega$  trim to achieve its performance. This adjustment is set in accordance with the notes in Figure 2 and centers the AGC's capture range.

## OSCILLATOR DISTORTION

Verifying oscillator distortion necessitates sophisticated measurement techniques. You will encounter limitations if you attempt to measure distortion with a conventional distortion analyzer, even a high-grade type. An oscilloscope can be used to indicate distortion residuals at the analyzer's output (Figure 4). The amplifier's floor faintly outlines noise and uncertainty on any signal activity that relates to the oscillator.

The Hewlett-Packard (www.hp.com) HP-339A analyzer specifies a minimum measurable distortion of 18 ppm. The figure shows the instrument indicating 9 ppm, which is beyond the unit's specification and, hence, highly suspicious. Measuring distortion at or near the limits of your equipment yields pronounced uncertainties. Distortion measurements at or near equipment limits are full of unpleasant surprises (Reference 1).

Specialized analyzers with low uncertainty floors are needed to meaningfully measure oscillator distortion. The Audio Precision (www.ap.com) 2722 analyzer has a maximum 2.5-ppm THD+N (total harmonic distortion plus noise) and a typical THD+N of 1.5 ppm. This instrument measures the oscillator's THD in three tests and finds THD figures of -110, -105, and -112 dB at 3, 5.8, and 2.4 ppm, respectively (Figure 5). These measurements provide confidence in applying the oscillator to ADC-fidelity characterization.



**Figure 6** A partial display of the test system includes time-domain information, a Fourier spectral plot, and detailed tabular readings for an LT6350-driven ADC.



## ADC TESTING

When you test ADCs, you route the oscillator's output to the ADC through its input amplifier. The test measures distortion products produced by a combination of the ADC and the ADC's input amplifier. You then examine the ADC's output with a computer, which quantitatively indicates spectral-error components (**Figure 6**).

You can download the code to take measurements and obtain input-amplifier, ADC, computer-data-acquisition, and clock boards from the Linear Technology Web site. Appropriate parts include an oscillator; the Linear Technology LT6350 amplifier; the LTC1279 ADC; the DC718 interface card; and any stable, low-phase-noise, 3.3V clock capable of driving 50 $\Omega$ .

The computer display includes time-domain information showing the biased sine wave centered in the converter's operating range. It also displays detailed tabular readings and a Fourier transform indicating spectral-error components. The amplifier/ADC combination under test produces second harmonic distortion of -111 dB, which is approximately 2.8 ppm. The higher-frequency harmonics are well below this level, indicating that the ADC and its input amplifier are operating properly and within specifications. Harmonic cancellation may occur between the oscillator and amplifier/ADC combo, mandating that you test several amplifier/ADC samples to enhance your confidence in the measurement. **EDN**

## REFERENCE

1 Williams, Jim, "Bridge Circuits: Marrying Gain and Balance," Application Note 43, Linear Technology, June 1990, <http://bit.ly/pF8qsv>.

## AUTHORS' BIOGRAPHIES



Jim Williams was a staff scientist at Linear Technology Corp, where he specialized in analog-circuit and instrumentation design. He served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology. He was a former student at Wayne State University (Detroit) and enjoyed sports cars, art, collecting antique scientific instru-

ments, sculpture, and restoring old Tektronix oscilloscopes. A long-time EDN contributor, Williams died at age 63 in June 2011 after a stroke.

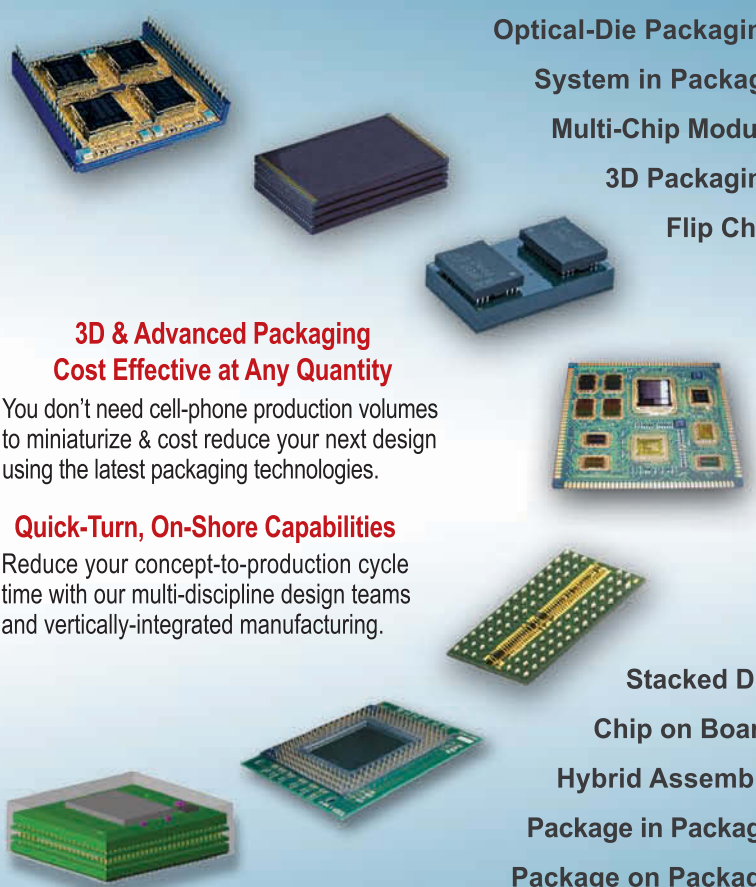


Guy Hoover is an applications engineer at Linear Technology Corp in the mixed-signal-products group supporting SAR (successive-approximation-register)

ADCs. He has a bachelor's degree in electronics-engineering technology from DeVry Institute of Technology (San Francisco, CA). Hoover has written several application notes and articles. His hobbies include watching classic sci-fi movies and collecting high-tech gadgets.

 Read more articles by Jim Williams at [www.edn.com/jimwilliams](http://www.edn.com/jimwilliams).

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# SOCs:

# IP IS THE NEW

BY RON WILSON • EDITOR-AT-LARGE

**REUSABLE IP, NOT  
SYSTEM-LEVEL  
LANGUAGE, HAS  
BECOME THE  
NEW LEVEL OF  
ABSTRACTION.**

**T**o deal with increasing complexity, you must increase your level of abstraction. So goes the truism. But as Moore's Law accelerates the complexity of SOCs (systems on chips) toward escape velocity, where do you find a new abstraction to supplement RTL (register-transfer

level)? Many observers, noting that textual, hardware-oriented RTL replaced schematics, argue by analogy that a system-description language, such as SystemC, will provide the next great abstraction. That scenario didn't happen, however.

"Reusable IP [intellectual property] is the new level of abstraction," says Ajoy Bose, chairman, president, and chief executive officer of Atrenta. If you examine what SOC-design teams are doing, you'll find that creating an SOC is a process of finding, characterizing, and assembling previously used IP. Design-creation tools, whether SystemC, Verilog, or schematics, find a role only in filling in the blanks—the proprietary functions and connective tissue of the IC. But today's design flows, as broad-spectrum-EDA companies, the foundries, and most SOC designers conceive them, have been slow to recognize this reality. Look at your tools, and you would think that every SOC begins with a set of functional requirements and a clean sheet of paper. Instead, consider what really goes on in an SOC design and what conclusions you can extract from these observations.

# Abstract Construction



IMAGE: © MATTHIAS KULKA/CORBIS



## THE NEW ABSTRACTION

Synopsys Chairman and Chief Executive Officer Aart de Geus likes Legos. At least, he likes to use them as an analogy for silicon IP. He points out that fitting together IP to create an SOC has its similarities to fitting together Lego blocks to build a toy. IP blocks are abstractions of the RTL inside them, just as Lego blocks are far simpler than crafting a spaceship or a dinosaur from wood or plastic. You can run a long way with the analogy before it begins to break down.

Legos, especially the elaborate pieces in the expensive theme sets, can also illustrate what an IP-centric design flow must look like. You start out with requirements, as in a traditional flow. But the IP-centric flow immediately departs from tradition. In the traditional flow, you partition the requirements into ever-smaller modules, carefully defining interfaces as you go, until the modules are small enough that

## AT A GLANCE

➤ Reusable IP (intellectual-property) blocks have become the new level of abstraction for SOC (system-on-chip) design.

➤ An ideal IP-assembly flow would let SOC designers simply put blocks together without opening them.

➤ The gating achievement in the automation of the IP-centric flow may be increasing standardization and craft in the creation of the IP.

your RTL designers can write them in Verilog. But an IP-centric flow is almost the opposite: You select available IP blocks and fit them into the requirements, as you would assemble a Lego kit. You try to use as few blocks as possible and leave as few holes as you can. You then fill in the holes with new code.

Moving down the design flow, the two approaches continue to diverge. Through functional verification; syn-

thesis; analysis; detailed clock, power, and test insertion; back-end design; and closure, the traditional flow continuously removes abstraction, creating more implementation detail until the requirements have become layers of polygons. At each new level, the flow stops to verify that the design still meets the requirements.

The IP-centric flow, again, is nearly the opposite. The point is to assemble the IP into a system that meets the requirements and uncovers as little new information about the IP's entrails as possible. "Don't get stuck debugging the IP during the assembly process," says Bose.

That scenario is the ideal and, for many teams, attractive. "In China, for example, methodology is about how quickly you can go from definition to IP list to assembly," says de Geus.

That situation is often not the reality, however. "At least some functions today are so well-defined that you could

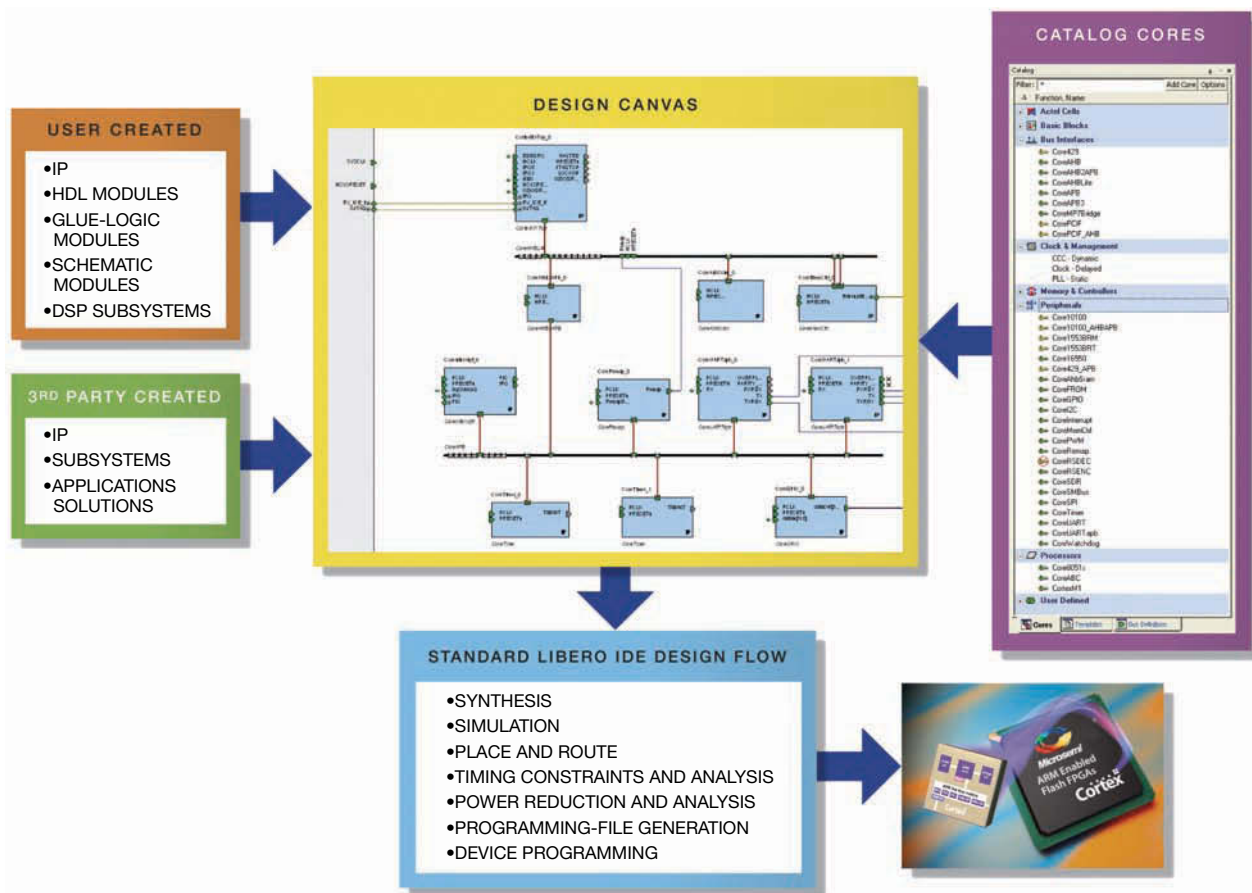


Figure 1 In a constrained environment, such as an FPGA, designers can assemble library IP directly into an SOC.

in principle treat them as black boxes all through the flow, but I have yet to see it," says Taher Madraswala, vice president of engineering at Open-Silicon. "In reality, you end up taking apart your black boxes in synthesis and gate-level optimization." To address these issues, you must walk through an ideal design flow, discovering the gaps between vision and reality. You must consider IP selection, assembly, implementation, and closure.

## IP SELECTION

The move from requirements to an IP BOM (bill of materials) is variable and, unfortunately, manual. How you get from A to B depends on the nature of the system, the availability of IP, the design team's experience with reuse, marketing's plans for differentiating the chip, and corporate policies, among other things. The one thing the process does not depend on is automation.

Synopsys' de Geus points out that,

in principle, there should be no barrier to automation. At RTL, he observes, Design Compiler effectively infers relatively complex blocks of the company's DesignWare from the Verilog source. For larger IP blocks, however, automation is uneven. "With IP, the blocks are less generic, and more human selection is involved," he says.

In some cases, manual IP selection can approach the ease of an automated tool. For example, many smaller SOC's still adhere to a simple, microcontroller-like architecture: a CPU core, a local cache, and a collection of peripheral interfaces. All the blocks you need are often available from third-party IP libraries, complete with AMBA (advanced-microcontroller-bus-architecture)-interface pins, ready to plug together. In other cases, the choice of IP is not obvious from the requirements. Say, for example, that your smartphone SOC has several authentication and encryption requirements. Do

## AN FPGA VIEW

The first appearance of an IP (intellectual-property)-centric design flow was not in the ASIC business but in the FPGA world. All of the major FPGA vendors produced environments—IP libraries, standard interconnect buses, and GUIs (graphical user interfaces) driving automated assembly tools—that would produce simple SOC (system-on-chip) designs that were correct by construction, with virtually no RTL (register-transfer-level) involvement by the designers.

In Actel's (now Microsemi's) case, a GUI presents a canvas on which the designers can move and interconnect IP blocks, according to Rich Kapusta, vice president of terrestrial products at the SOC division of Microsemi. The IP can come from Microsemi's libraries or can represent the hard blocks in the company's FPGAs. The tool then instantiates blocks that create an AMBA (advanced-microcontroller-bus-architecture)-compliant fabric to interconnect the IP as the designer has requested.

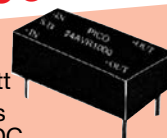
The library's contents now range from relatively simple functions to complete subsystems, much like commercial libraries for ASIC developers. Designers can add their own RTL blocks to these functions, they can put their own wrappers around the library blocks to enhance their performance, or they can delve into the library blocks at RTL and modify them, generally with Microsemi's assistance.

At the densities involved, Kapusta says, designers usually do verification at the system level by simply programming and trying some parts. The relative simplicity of the designs and the rigorous construction process minimize the possibility of design errors to the point that debugging a newly assembled chip is a manageable problem. So, in one world, at least, there are enough constraints that the ideal of the IP-centric flow has become a practical reality.

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you license a large and expensive third-party cryptographic engine or choose a smaller cryptographically oriented datapath coprocessor? Alternatively, do you develop your own block in The MathWorks' Matlab and synthesize it, or do you get a faster—or a second—CPU core and handle the requirements in software?

Choosing a function does not end the process. Functionally similar blocks can differ in many ways, including performance, area, power, interface requirements, configurability, provisions for clock and power controls, verification coverage, and use history. Much of this information should be on the IP block's data sheet, but some may require interrogating previous users of the block or even a bit of reverse-engineering.

The logical problem of inferring a complex IP block from an executable SOC-requirements file is probably solvable. Most requirements documents are

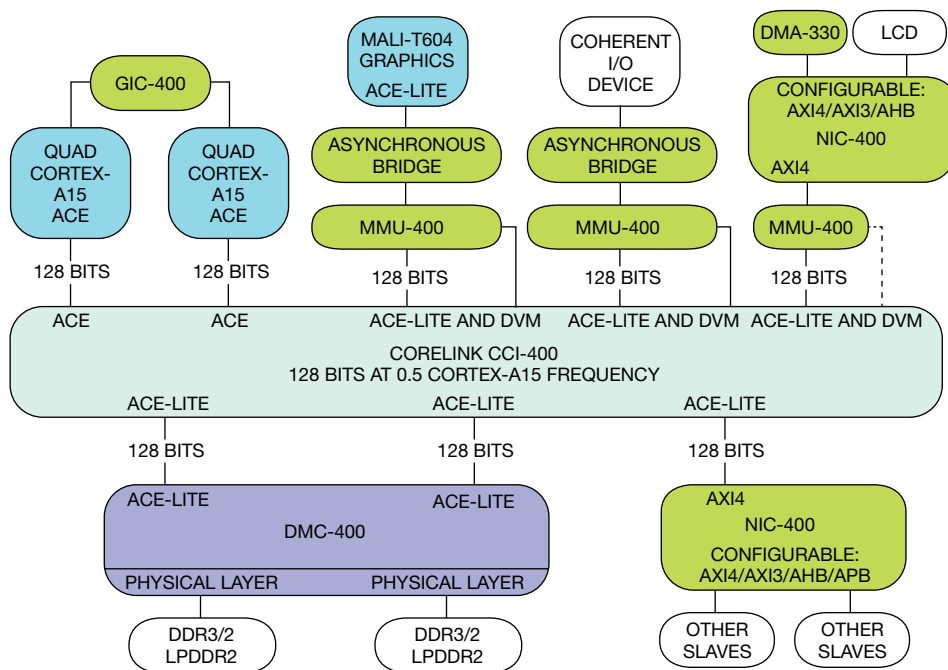
still in human languages, not executable form, however. Further, most of the supporting information necessary for selecting a piece of IP is scattered, lacks standard formats, and may be proprietary. Clearly, automating IP selection requires a lot of work.

One intriguing, largely unexplored possibility exists. You normally think of formal verification as involving verification tools. The ability to formally test the truth of a property has applications outside traditional verification, however, according to Oz Levia, vice president of marketing and business development at Jasper Design Automation. For example, designers can use Jasper's ActiveDesign to explore RTL during development, helping to steer RTL-code creation. Extending this idea, Levia describes how Jasper and ARM engineers teamed to manually convert the English-language specification for ARM's memory-coherency protocol

into an executable spec, from which Jasper synthesized a set of assertions. In principle, a design team could use this process to create a set of assertions from requirements and then use a formal tool to investigate how nearly an IP block fits the requirements. Programmable or configurable IP would create challenges, but the procedure might at least generate a statement of work for fitting a block of IP into a design.

## ASSEMBLY

IP assembly is the essence of the IP-centric flow. Some designers use the word "assembly" instead of "integration" to make an important distinction. The ideal at this stage is to treat the IP blocks as configurable black boxes, writing only the RTL that is necessary to glue the boxes together after you have configured them. This situation differs greatly from the increasing exploration of the blocks



ACE: ARM CPU ESTIMATOR  
AHB: ADVANCED HIGH-PERFORMANCE BUS  
APB: ADVANCED PERIPHERAL BUS  
AXI: ADVANCED EXTENSIBLE INTERFACE  
CCI: CACHE-COHERENT INTERCONNECT  
DMA: DIRECT-MEMORY ACCESS  
DMC: DYNAMIC-MEMORY CONTROLLER

DVM: DISTRIBUTED VIRTUAL MEMORY  
GIC: GENERIC INTERRUPT CONTROLLER  
I/O: INPUT/OUTPUT  
LCD: LIQUID-CRYSTAL DISPLAY  
LPDDR: LOW-POWER DOUBLE DATA RATE  
MMU: MEMORY-MANAGEMENT UNIT  
NIC: NETWORK-INTERFACE CARD

**Figure 2** Vendors are now building SOCs by attaching cores to a standard interconnect fabric, such as ARM's AMBA AXI (advanced extensible interface).



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that the word "integration" implies.

The ideal assembly process necessarily begins with system-level simulation. In another sense, system simulation is the verification phase of IP selection; you are proving that the pieces you selected can come together in a way that will meet the system requirements. "In an IP-assembly flow, system verification and validation get massively more emphasis," says de Geus. "Often, you need a rapid prototype just to prove that the software will run on the chip."

The importance of rapid prototyping implies that transaction-level models of IP blocks can be valuable. But the IP vendor sometimes doesn't have transaction-level models, or the models are no longer correct for the current version of the IP. You can nearly always use the soft IP's RTL source, though, to create an FPGA-based rapid prototype—hence the importance of FPGA prototyping to IP-centric design.

You can also make other early assessments during assembly. Static analyzers can check the IP for rules violations and best-practices compliance. Estimators can often come reasonably close on power, performance, and area of the finished chip. "Today, there is more uncertainty about the results using high-level synthesis than using soft IP," says Atrenta's Bose.

In an ideal world, once you have put the blocks together in the prototype, verified the behavior of the system, and explored its probable characteristics, the only verification you would need to do would be of the connective tissue between the existing blocks and of the new blocks. But different situations approach this ideal to differing degrees.

Perhaps the closest approach to

ideal is when the IP, the interconnect, and the IC implementation all come from one source (Figure 1). For one example of this situation, see sidebar "An FPGA view." This good fortune does occur in real life, but only in vertically integrated companies with strong design-reuse cultures, such as IBM, parts of STMicroelectronics, several of the major Japanese companies, and both NXP and Freescale before private-equity ownership refocused their priorities. Without both a strong corporate reuse culture and firm control over the IP-development process, it is difficult to get close to a pure black-box assembly flow. "People still tend to lag on the little bit of extra work necessary to enable reuse," says Bose, who states that Japan's STARC (Semiconductor Technology Academic Research Center) produced an excellent reuse manual. Some teams that develop IP lack both the discipline and the management support to make their design reusable at this level, however.

The next closest to an ideal environment is one in which an industry standard, such as AMBA, defines all the interconnect between the blocks, and all the IP complies with the standard (Figure 2). In this case, assembly is a matter of making sure signal names and polarities agree and that all the interfaces can operate at the desired frequencies.

Without a unifying bus standard, things get more complex. You have to understand the interfaces on the instances of configured IP blocks and, if necessary, create additional RTL glue to execute transactions between the blocks, and you must verify all of this work.

The art, according to Open-Silicon's Madraswala, is to find a way to verify the interactions without verifying all the internals of the IP. "You can exploit the fact that the IP has been used before," he says. "You look at your schedule and determine where you want to spend your verification time. You might write assertions or tests to verify the logical integration requirements in the IP data sheet, rather than doing a full verification plan. But experience is vital in knowing what you do and don't have to check." This verification approach relies heavily on simulation rather than formal tools, Madraswala adds.

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## IMPLEMENTATION

At this point, the IP-centric design flow begins to reconverge with tradition. Soft IP blocks, new blocks, and interconnect all go through synthesis and on to scan insertion, place, and route. Hard IP also enters the flow for placement and routing. The team then closes the design. In some respects, however, the IP-centric design remains distinct.

One difference, Madraswala says, is the approach to power management. "Tuning the design for power management is becoming a separate phase of the design flow," he says. "It is becoming its own art and science." Madraswala explains that, when you've designed a block yourself, you can use synthesis switches for reregistering to ease timing; for fine-grained clock gating; and for other netlist-level-optimization techniques, most of which benefit power consumption.

Other tools can, for example, alter clock skews to manage peak clock currents. You can do some of this work with synthesis switches, but engineers still manually perform some of these tasks, according to Tobias Bjerregaard, chief executive officer at Teklatech. All of these techniques can be valuable, but it may not be wise to use them all with third-party IP.

"We may not have the original source code, so we can't do equivalence checks," says Madraswala. "Often, we don't have the right to change the design of the block." The question of how much optimization a licensee can do before violating the terms of the warranty on an IP block is difficult.

Synopsys' de Geus is also skeptical about relying on equivalence checkers—for a different reason. "The formal tools are constantly chasing what synthesis can generate," he says. "For instance, the synthesis tools can do delay borrowing, but the formal equivalence checkers may not see the reorganized circuit as equivalent to the original."

Consequently, Open-Silicon's Madraswala suggests applying clock and power gating to IP at the block level. "We put a wrapper around the code and make it behave the way we want it to," he explains. This approach avoids modifying the third-party code. Physical design, Madraswala says, remains traditional. Hard-IP blocks join the flow for placement and routing, relying on

the vendor's integration guidelines. The company runs a DRC [design-rule check] on the block to ensure that it complies with the current rule deck and performs a visual review of the integration with the vendor, according to Madraswala. "Sometimes, there are guidelines that they haven't written down," he says. Open-Silicon follows this process with a DRC of the flattened design, but Madraswala claims that no problems exist 99% of the time.

## THE GENIUS IN LEGOS WAS HALF IN MAINTAINING TIGHT TOLERANCES SO THAT THE PLUGS AND SOCKETS WOULD WORK.

The back-end flow benefits relatively little from IP-based design. Except for FPGA designs, you cannot ignore DRC, extraction or timing, signal-integrity, and power-integrity closures. Too much art and too many details, such as different constraints, power-management strategies, and approaches to DFT (design for test), remain in these areas. These differences may show up only in the integrated chip. Yet, the ideal of an IP-centric design flow—selecting and snapping together blocks, verifying the interconnect, and pushing a button to get a finished design—remains.

Such a flow would require great discipline from IP designers. "The genius of Legos was only half in thinking of the plugs and sockets," says de Geus. "The other half was figuring out how to maintain the very tight tolerances so that the plugs and sockets would work over and over again, without jamming or loosening up." And so it is with further automation of the IP-centric flow: The gating achievement may be increasing standardization and craft in the creation of the IP. **EDN**

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# Build an electric vehicle from the ground up

FRUSTRATED BY FAST-RISING GASOLINE PRICES, JOHN SANTINI, VICE PRESIDENT OF ENGINEERING AT TDI POWER, DECIDED TO TURN HIS CREATIVITY AND PROBLEM-SOLVING SKILLS TOWARD DEVELOPING HIS OWN ELECTRIC VEHICLE.

**E**Vs (electric vehicles) and HEVs (hybrid electric vehicles) are advancing rapidly. Such vehicles include the Toyota Prius, the highest-selling hybrid; the Ford Fusion, with 41-mpg city mileage; the Chevy Volt, with 35-mile stretches of all-electric driving; and the Nissan Leaf, the first affordable, mainstream, all-electric five-passenger car.

Another, perhaps lesser-known, EV uses the front suspension and steering gear from a 1988 Pontiac Fiero donor car. The man responsible for this ground-up design is John J Santini, vice president of engineering at TDI Power ([www.tdipower.com](http://www.tdipower.com)), a company that has been in the power-conversion industry for more than 50 years and has been providing power equipment in mobile, hybrid, and EV applications for more than 25 years. Frustrated by fast-rising gasoline prices, Santini turned his creativity and problem-solving skills toward developing his own EV.

## THE PROJECT

Although Santini's original goal was to build a plug-in hybrid vehicle, the fast-falling cost of lithium-ion batteries spurred the decision toward the end of the project to postpone the engine/generator and to add some weight back in as additional lithium-ion batteries. As a result, the current vehicle is all-electric, although the space remains to add an engine generator in the future. Doing so will increase the cruising range of the vehicle well beyond the 90-mile range of the current system. The total vehicle weight, with batteries, is now 2050 lbs.

The project is a lightweight, two-seat commuter car. The frame is a space-frame design, inspired by the Locost project cars and similar-construction vehicles. A Locost is an economical, home-built Clubman-style sports car employing the concept of the original Lotus 7. Two books provide guidance on how to construct your own Locost (**references 1 and 2**). Santini was also inspired, in part, by a Cornell University EV built in 1975.

The body is a custom design, fitted around the frame, made of 1-in.-thick Styrofoam covered with one to three layers of 0.009-in.-thick fiberglass cloth and epoxy. Technically, it's a three-wheeler because the rear wheel is a solid assembly with two tires and the drive pulley in the center. The belt drive is more than 99% efficient, whereas even a simple two-speed transmission would likely incur losses of as much as 10%.

## BATTERY CHARGER

The battery charger comprises a pair of 54V, 80A TDI Mercury chargers—one for the lower 48V and one for the

upper 48V pack, with 120/240V-ac input—in series with the battery's center tap to keep the batteries balanced (**Figure 1**).

At 4.3 kW, the TDI Mercury battery chargers perform a typical bulk charge in less than one hour, and there is plenty of time to soak up a full charge during the day. The original chargers were only 1.2-kW Mercury units that charged at 30A. Charging used to take all day at work because just “topping off” the battery required four hours.

Santini has also added a new circuit that detects battery current greater than 60A and turns on the brake lights. The regenerative braking is turned up high, so when you fully back off the gas pedal, braking is strong. Santini rarely uses the hydraulic-brake system, so he has noticed some surprised drivers very close to his car's rear end!

Plans are afoot to lower this charge to 30A so that the twin rear brake lights and rear-window brake lights go on under almost all regenerative-braking conditions; this modification requires merely a change in the threshold to an onboard comparator. Santini has also converted the taillights to LED to use less energy and to be fast-acting and brighter (**Figure 2**).

The mechanical braking system in this car should last for more than 150,000 miles because a driver typically needs to use it only at stop signs or traffic lights on an incline, after regenerative braking has taken effect, to stop any rolling.

## AC MOTOR AND AC-MOTOR CONTROLLER

The ac motor from ABM Greiffenberger ([www.abm-drives.com](http://www.abm-drives.com)) is rated at 18.7 kW, almost as much power as the old GE motor Santini had in his electric-Corvette design in 1975. It



**Figure 1** The vehicle uses two TDI Mercury battery-charging converters in series with the battery's center tap.





**Figure 2** Fast-acting LED brake lights are bright and energy-efficient.



**Figure 3** The drive uses a single 62-mm-wide gear belt with a single reduction of approximately 6.3-to-1.

weighs only 165 lbs, and, with an 84V input, it operates at constant torque to as much as 3000 rpm and then constant horsepower to as much as 6000 rpm. The drive uses a single 62-mm-wide gear belt with a single reduction of approximately 6.3-to-1 (**Figure 3**).

The Curtis ([www.curtisinstruments.com](http://www.curtisinstruments.com)) ac-motor controller is a new model that works well with a 96V-nominal battery

pack. It has all the features necessary for a complete vehicle controller, including regenerative braking. It is rated at 60 kW (80 hp) with this battery/motor combination. The finned heat sink has ducted air through it from the body-side air intake in this all-air-cooled vehicle (**Figure 4**).

### LEAD-ACID VERSUS LITHIUM-ION BATTERIES

The original batteries were lead-acid, weighing 800 lbs. However, over the three-year span of the project, the cost of lithium-ion batteries halved, and their cycle life doubled. The new 350-lb lithium-ion batteries from Thunder Sky ([www.thunder-sky.com](http://www.thunder-sky.com)) comprise 30 200-Ahr cells forming a 100V, 200-Ahr pack (20 kWhr), which gives an approximately 90-mile range.

Santini does not have a battery-balancing circuit, but the cells stay in balance when they are new. Stay tuned for the next steps for further improvements (**Figure 5**).

Lead-acid batteries have a high surge-to-weight ratio, meaning that they can deliver a big jolt of electricity all at once. This feature makes them work well in applications that need a big, sudden surge of power, such as car starters. The batteries are also inexpensive to produce. On the downside, lead-acid batteries tout one of the lowest energy-to-weight and energy-to-volume battery designs, making them big and heavy for the total amount of power they can put out. They also perform poorly in roles that require a steady, low, or mid-

## BUT WAIT: THERE'S MORE!

*By Patrick Mannion, Director of Content*

This feature is **Part 1** of a two-part series that appears online at [EDN.com](http://EDN.com). **Part 1** discusses the genesis of the EV (electric-vehicle)-development project, the motor-control and power-management functions, lead-acid versus lithium-ion batteries, and the author's test drive. View **Part 1** in its entirety online at <http://bit.ly/oEor0D> and find links to several related videos.

**Part 1** clearly resonated with you, given the many enthusiastic and inquiring responses online—everything from descriptions of readers' attempts to build their own EVs to interactive discussions with John Santini, vice president of engineering at TDI Power, including one on EV-motor design and selection. For example, in the online responses, TedC asks: "So, when can we expect the rest of the story?" Ted, we're happy to say that you can now find **Part 2** at <http://bit.ly/r1wSx4>. In this continuation of the story, which includes tons of additional photos, the author gets into the real details of the design—from components, mechanicals, frame construction, specifications, and performance charts to why he had to break down his basement wall. Enjoy!



**Part 2** of this article explains why the author had to wreck his basement wall to complete the project.



**Figure 4** The Curtis ac-motor controller gives 80 hp with the battery/motor combination.



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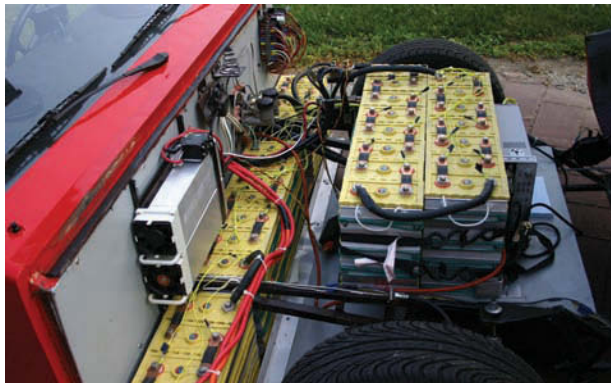
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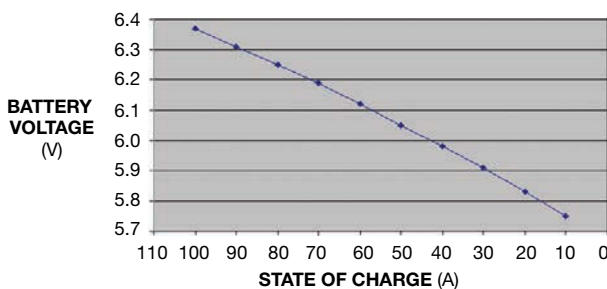
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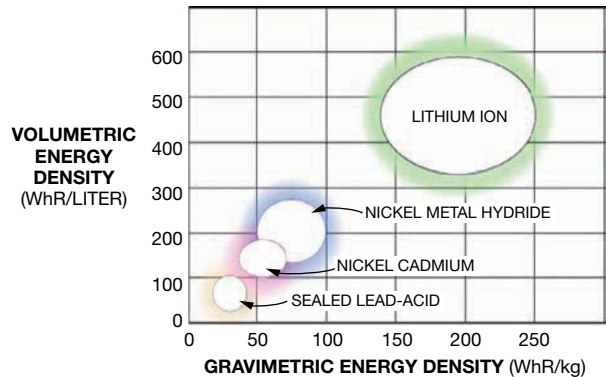




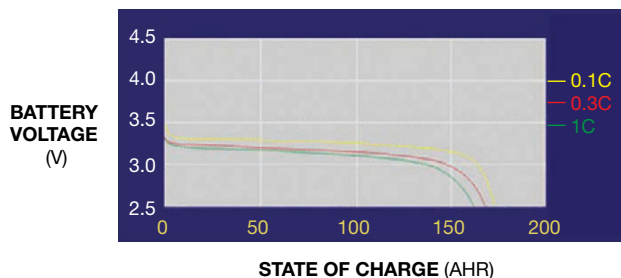
**Figure 5** New 20-kWhr lithium-ion batteries each have a wire running to a data logger, so you can monitor all of the cells during both charge and discharge.



**Figure 7** The X axis of a 6V lead-acid-battery-discharge curve shows state of charge, and the Y axis shows battery voltage (courtesy Trojan Battery Co, [www.trojanbattery.com](http://www.trojanbattery.com)).



**Figure 6** Lithium-ion batteries are lighter and smaller than lead-acid devices and have higher energy density (courtesy Micro Power Electronics, [www.micro-power.com](http://www.micro-power.com)).



**Figure 8** Lithium batteries have a fairly flat discharge curve with sharp shoulders (courtesy EnerDel, [www.ener1.com](http://www.ener1.com)).

dling supply of electricity over a long period of time, and they have long recharging times.

Lithium-ion batteries, on the other hand, have high power-to-weight and power-to-volume ratios, so they are lighter and smaller than lead-acid types. Special types of lithium-ion devices have high surge capacity, but those types are more expensive. Regardless, an EV does not need “cranking” power to start, as a gas-powered vehicle does. The ac motor draws higher currents only during acceleration. Lithium-ion batteries also do not require frequent maintenance, as lead-acid types do (**Figure 6**). **Figures 7** and **8** show discharge curves for lead-acid and lithium-ion units, respectively.

## HOW IT DRIVES

Santini allowed me drive the car so that I could convey to EDN’s audience the feel of an EV and describe the differences from a gasoline-engine vehicle (see **sidebar** “But wait: There’s more!”). When I started up the vehicle with the key, I expected to hear the engine-cranking noise that you would hear in a gasoline-powered vehicle’s starter, but there was only silence. The dashboard lights came on, and the panel meters came to life. When I put the vehicle in reverse to back out of the parking space, the “forward/reverse” stick was on the center console as I expected, but Santini explained that this stick was only for driver familiarity. He originally had planned to put a toggle switch or a similar device on the dashboard panel because that is all the ac-motor controller needs to reverse

the motor direction; there is no transmission in this vehicle.

Because an ac motor drives the vehicle using a belt, the only sound heard when driving is the whine of the drive belt. This sound begins to dissipate at high speeds. The top speed is 70 mph. I took a corner at more than 40 mph at Santini’s suggestion, without any braking, and the vehicle held the road well. The battery’s upfront weight provides some good traction.

As for the braking system, it takes a couple of times before you are comfortable with the fact that the braking is adequate to stop the car by just backing off the accelerator. I got used to it after three or four times. **EDN**

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## AUTHOR’S BIOGRAPHY



Stephen Taranovich has 40 years of experience in the electronics industry. He received a master’s degree in electrical engineering from the Polytechnic Institute of New York University (Brooklyn, NY) and a bachelor’s degree in electrical engineering from New York University (Bronx, NY). He is chairman of the Educational Activities Committee for IEEE Long Island.



# Are you violating your op amp's input common-mode range?

UNDERSTAND THIS CRITICAL OP-AMP PARAMETER AND HOW IT CAN BE THE SOURCE OF MYSTERIOUS MISBEHAVIOR AND INCONSISTENT PERFORMANCE.

You go through a process to select an operational amplifier for your circuit by considering the most critical parameters of your application. Some of the parameters you review may include supply voltage, gain-bandwidth product, slew rate, and input noise voltage. You also must account for input common-mode range, a key parameter important for all op-amp circuits.

Engineers who have worked with op amps throughout their careers likely have experienced situations in which an op amp was behaving in an unexpected manner. The nice thing about op amps is that their outputs often tell the story. In many cases, if something is not right, it shows up in an obvious way at the output pin. Limitations at the output stage can cause undesirable output waveforms. Perhaps too much capacitance on the output is causing an oscillation, or clipping occurs before reaching the full rail voltage because the output stage's voltage swings are less than the supply-rail voltage.

Strange behavior can also appear at the op amp's output that has nothing to do with the output stage. The undesirable output signal may result from something wrong at the input side of the device. One of the most common issues with op amps is a violation of the device's input common-mode range.

## INPUT COMMON-MODE VOLTAGE

$$V_{ICM} = \frac{V_{IN+} + V_{IN-}}{2}$$

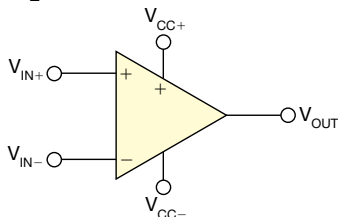


Figure 1  $V_{ICM}$  describes a voltage level and is the average voltage at the inverting and noninverting input pins.

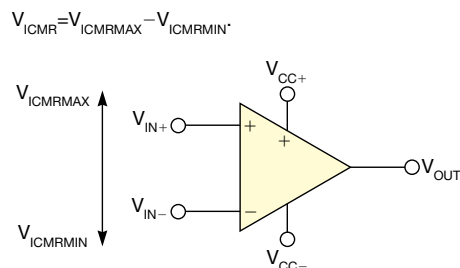


Figure 2  $V_{ICMR}$  is a range that minimum  $V_{ICMR}$ ,  $V_{ICMRMIN}$ , and maximum  $V_{ICMR}$ ,  $V_{ICMRMAX}$ , describe.

But what exactly is input common-mode range, and what is the impact of violating or exceeding it?

Input common-mode voltage,  $V_{ICM}$ , is one of the first specifications an engineer thinks of when considering op-amp inputs, but it may lead to some initial confusion.  $V_{ICM}$  describes a voltage level and is the average voltage at the inverting and noninverting input pins (Figure 1). It is commonly expressed using the following equation:

$$V_{ICM} = [V_{IN+} + V_{IN-}] / 2$$

Another way to think of  $V_{ICM}$  is that it is the voltage level common to both noninverting and inverting inputs,  $V_{IN+}$  and  $V_{IN-}$ . In most applications  $V_{IN+}$  is very close to  $V_{IN-}$  because closed-loop negative feedback causes one input pin to closely track the other such that the difference between  $V_{IN+}$  and  $V_{IN-}$  is close to zero. This situation is true for many common circuits, including voltage followers and inverting and noninverting configurations. In these cases, you commonly assume that  $V_{IN+} = V_{IN-} = V_{ICM}$  because these voltages are approximately the same.

Another term to describe op-amp inputs is input common-mode range,  $V_{ICMR}$ , or, more correctly, input common-mode voltage range. Data sheets most often use this parameter, and

**TABLE 1**  $V_{ICMR}$  EXAMPLES

Device	Technology	Maximum supply range: split-supply/single-supply limitations (V)	$V_{ICMRMIN}$ (V)	$V_{ICMRMAX}$ (V)
TLE2062A	JFET input	$\pm 19/38$	$(V_{CC-})+3.4$	$(V_{CC+})-1$
TLC2272	LinCMOS	$\pm 8/16$	$(V_{CC-})-0.3$	$(V_{CC+})-0.8$
TL971	BiCMOS	$\pm 7.5/15$	$(V_{CC-})+1.15$	$(V_{CC+})-1.15$
OPA333	CMOS/rail-to-rail input	$\pm 2.75/5.5$	$(V_{CC-})-0.1$	$(V_{CC+})+0.1$
OPA735	CMOS	$\pm 6/12$	$(V_{CC-})-0.1$	$(V_{CC+})-1.5$

it is the one that circuit designers should be most concerned about.  $V_{ICMR}$  defines a range of common-mode input voltages that results in proper operation of the op amp and describes how close the inputs can get to either supply rail.

Another way to think of  $V_{ICMR}$  is that it describes a range that minimum  $V_{ICMR}$ ,  $V_{ICMRMIN}$ , and maximum  $V_{ICMR}$ ,  $V_{ICMRMAX}$ , describe, as the following equation shows:

$$V_{ICMR} = V_{ICMRMAX} - V_{ICMRMIN}$$

where  $V_{ICMRMIN}$  is the limit relative to the  $V_{CC-}$  supply rail and  $V_{ICMRMAX}$  is the limit relative to the  $V_{CC+}$  supply rail (Figure 2).

When the op amp exceeds  $V_{ICMR}$ , the device may not perform normal linear operation. Therefore, you must understand the entire range of the input signal and ensure that the op amp does not exceed  $V_{ICMR}$ .

Another point of confusion may be that  $V_{ICM}$  and  $V_{ICMR}$  are not standard abbreviations, and various data sheets from various IC suppliers often use different terminology, including  $V_{CM}$ ,  $V_{IC}$ , and  $V_{CMR}$ . Consequently, you must understand that the specification you're looking for is more than a particular input voltage; it is an input voltage range.

### $V_{ICMR}$ VARIES AMONG OP AMPS

An op amp's design specifications and the process technology it uses dictate the device's input stage. For example, the input stage of a CMOS op amp differs from that of a bipolar op amp, which differs from that of a JFET op amp. It is important to note that these differences exist among various op amps.

Table 1 shows several examples of Texas Instruments op amps and their  $V_{ICMR}$ . The maximum-supply-range column

describes split- and single-supply limitations. From the table it is clear that the input range,  $V_{ICMR}$ , differs from op amp to op amp. Depending on the type of device,  $V_{ICMR}$  may fall within or beyond the supply rails. Hence, never assume that an op amp can receive a specific input signal range until you verify it in the data-sheet specifications.

**$V_{ICMR}$  MAY FALL WITHIN OR BEYOND THE SUPPLY RAILS. NEVER ASSUME THAT AN OP AMP CAN RECEIVE A SPECIFIC INPUT SIGNAL RANGE UNTIL YOU VERIFY IT IN THE DATA-SHEET SPECIFICATIONS.**

One special case worth mentioning for wide input ranges is the rail-to-rail-input op amp. Although the name implies an op amp whose input can span the entire supply-rail range, not all rail-to-rail-input devices cover the entire supply range, as you might assume. Many rail-to-rail-input op amps, such as TI's OPA333, do span the entire supply range, but others fall short and are misleading in their description. Again, it is critical to review the specified input range in the data sheet.

### EXAMPLES OF VIOLATING $V_{ICMR}$

Violations of  $V_{ICMR}$  commonly occur in single-supply op-amp applications using 3.3V, 5V, or other low-voltage supplies. In these applications, the input signal range typically is narrow, and you must understand the input signal and  $V_{ICMR}$  to ensure proper op-amp operation. An op amp that violates  $V_{ICMR}$  can have undesirable output behavior, such as clipping the signal at voltage levels lower than you expect, voltage shifts in the output signal, phase reversal, or the output's prematurely reaching one of the supply-rail voltages.

To better understand the effects of exceeding  $V_{ICMR}$ , some examples with violations follow. Two op amps with different  $V_{ICMR}$  specifications demonstrate these effects. These devices have rail-to-rail outputs to rule out limitations due to the output stage. A single-supply voltage-follower circuit is used to evaluate both devices (Figure 3). All tests took place on a lab bench at a room temperature of approximately 25°C.

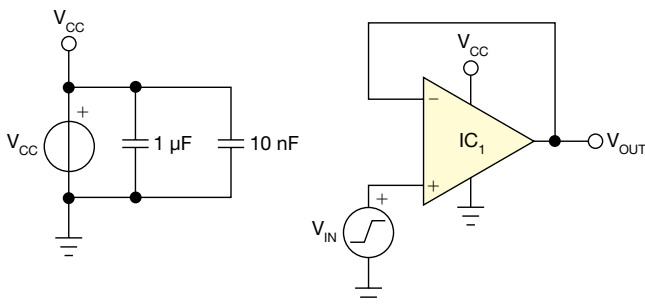


Figure 3 A single-supply voltage-follower circuit is used to evaluate both devices.

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- Aristotle Onassis

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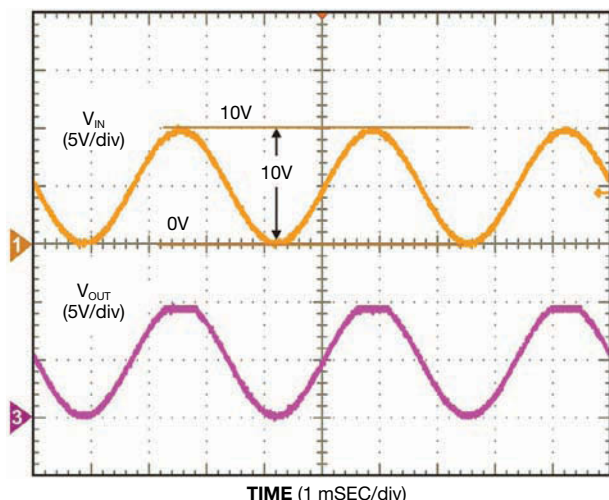
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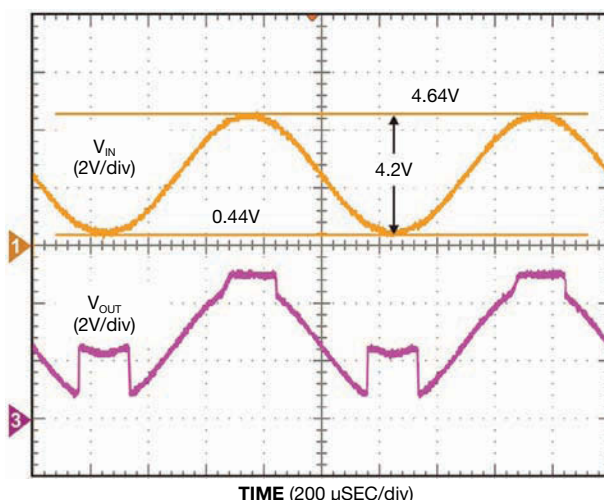
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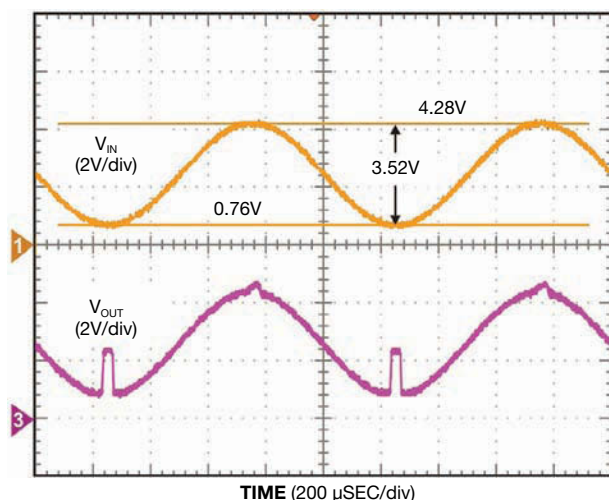




**Figure 4** The TLC2272's  $V_{OUT}$  shows clipping when  $V_{IN}$  (Channel 1) exceeds 9.2V.



**Figure 6** Nonlinear output behavior occurs when the TL971's  $V_{IN}$  is 4.2V p-p.



**Figure 5** Nonlinear output behavior begins when the TL971's  $V_{IN}$  is 3.52V p-p.

The first example uses a TLC2272 op amp with a  $V_{CC}$  of 10V. The data sheet describes its typical  $V_{ICMR}$  range as  $-0.3$  to  $+4.2$ V for a 5V supply voltage at  $25^{\circ}\text{C}$ . Note that the input limitation is near the positive supply rail, at 0.8V below  $V_{CC}$ . The resulting input limit near  $V_{CC}$  should be approximately 9.2V.

To test the circuit, apply a 300-Hz sine wave with a dc offset of half the  $V_{CC}$  voltage, or 5V, to the input. Adjust the ac amplitude until you see a change at  $V_{OUT}$ . When you apply 10V p-p input,  $V_{OUT}$  shows a clipped signal near the positive rail but not near the negative rail. This undesirable behavior near the positive rail is what you would expect if the input exceeds 9.2V. For  $V_{IN}$  of 0 to 9.2V,  $V_{OUT}$  shows a proper waveform, as you would expect (**Figure 4**).

The second example uses a TL971 rail-to-rail-output voltage-follower circuit but with different results. In this case, the op amp receives a single 5V supply. From the data-

## DIFFERENT NONLINEAR BEHAVIOR CAN RESULT FROM DIFFERENT OP AMPS WHEN THEY EXCEED $V_{ICMR}$ . PHASE REVERSALS OCCUR IN SOME BUT NOT ALL OP AMPS THAT VIOLATE $V_{ICMR}$ .

sheet specifications, the guaranteed  $V_{ICMR}$  range spans 1.15 to 3.85V, or roughly 2.7V p-p centered at  $V_{CC}/2$ . A 1-kHz sine-wave input is applied with a dc offset of 2.5V. Adjust the amplitude of  $V_{IN}$  from 200 mV p-p to larger levels until you see a change at  $V_{OUT}$ .

With  $V_{IN}$  centered at 2.5V,  $V_{IN}$  increases to 2.7V p-p with expected linear behavior at  $V_{OUT}$ . As  $V_{IN}$  increases to approximately 3.5V p-p, centered at 2.5V,  $V_{OUT}$  continues to follow  $V_{IN}$  and exhibits proper op-amp behavior. Note that the linear behavior is better than what you might expect from the data-sheet limits for  $V_{ICMR}$ , but it still exceeds the guaranteed limits. As  $V_{IN}$  increases slightly more to 3.52V p-p,  $V_{OUT}$  starts to exhibit nonlinear behavior near both the positive, 5V, and negative, 0V, rails (**Figure 5**).  $V_{IN}$  further increases to 4.2V p-p to clearly exceed  $V_{ICMR}$ . As the input peak exceeds the limit near the positive rail, the signal at  $V_{OUT}$  rails out as it jumps up to the positive rail, 5V, and stays there until  $V_{IN}$  returns to an acceptable range (**Figure 6**). As the input drops below the limit near the negative rail, the signal at  $V_{OUT}$  exhibits a phase reversal as it jumps to midrail, 2.5V, and tracks  $V_{IN}$  with an offset until  $V_{IN}$  increases to an acceptable voltage within the  $V_{ICMR}$ .

These examples show that different nonlinear behavior can result from different types of op amps when they exceed  $V_{ICMR}$ . Even though phase reversal results in the second case, note that phase reversals do not occur in every op amp that

violates  $V_{ICMR}$ ; it depends on the op amp.

The examples use an ac signal to evaluate  $V_{ICMR}$  for an op-amp circuit. Another useful test is to apply a dc-voltage source to the input of the circuit in **Figure 3**. While varying the dc input, the output level behaves in a similar manner, except that it doesn't vary over time. Depending on the type of circuit, ac analysis, dc analysis, or both may be useful in the early evaluation of the op amp.

### OVERCOMING A $V_{ICMR}$ ISSUE

What if you discover late in the design process that your op amp can't meet the  $V_{ICMR}$  requirements? The other device parameters may be ideal for your application, and it is difficult to change the device. You may want to consider one or more of the following options. First, if the input amplitude is too large, use a resistor divider to keep the signal within proper range of  $V_{ICMR}$ . Second, if the input signal offset is the problem, try using an input-biasing or dc-offset circuit to place the input signal within the specified  $V_{ICMR}$  range for the op amp. Third, you could try changing the device to a rail-to-rail-input op amp that meets all of your other requirements.

When selecting an op amp, remember that input common-mode voltage range is among the most critical specifications to understand. If the device's input cannot accept the levels or range of your input signal, you will likely experience problems at the output. Check this important detail first, and you'll thank yourself later when your circuit is operating properly. **EDN**

### ACKNOWLEDGMENT

This article originally appeared on EDN's sister site, Planet Analog (<http://bit.ly/quDfcQ>). The author wishes to thank Lucian Popa, a co-op student working at Texas Instruments while the author was writing this article. Popa assisted him in capturing the waveforms this article uses. The author also wishes to thank Art Kaye for his useful review and feedback.

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### AUTHOR'S BIOGRAPHY



Todd Toporski is a member of the technical staff at Texas Instruments, where he specializes in analog applications. He received a bachelor's degree in electrical engineering from Michigan Technological University (Houghton, MI) and a master's degree in electrical engineering from the Georgia Institute of Technology (Atlanta).

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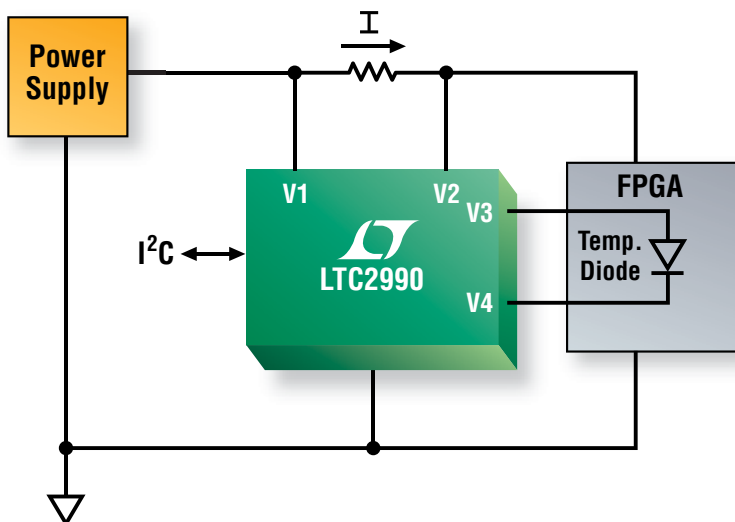
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1	x1	x1	x2			
2	x1	x1	x1	x2		
3	x1	x1	x1		x1	
4	x1	x1	x1			x1
5	x1	x1		x4		
6	x1	x1		x2	x1	
7	x1	x1		x2		x1
8	x1	x1			x2	
9	x1	x1			x1	x1
10	x1	x1				x2

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# designideas

READERS SOLVE DESIGN PROBLEMS

## Driver circuit lights architectural and interior LEDs

Steve Sheard, On Semiconductor, Tempe, AZ

LEDs are more efficient than incandescent lights and can last 100 times longer, but they require specialized electronic-drive circuits to avoid overstress conditions. The main operating parameter is relatively simple: Keep the current through the LEDs constant and under the specified maximum.

Traditional power supplies have accurate voltage outputs with variations in current. A resistor in series with an LED string controls the current. Such a design assumes a known voltage across the LEDs that does not vary with changes in LED temperature. Unfortunately, LEDs' forward voltage does change with temperature. LED manufacturers generally bin their devices by forward voltage, allowing a lighting manufacturer to build a lighting fixture to match this forward voltage at a fixed temperature. A circuit using unbinned LEDs saves the LED manufacturer time and results in less expensive LEDs. LEDs also have a negative forward-voltage-to-

temperature coefficient that can cause the drive circuit to go into thermal run-away, requiring the designer to build safeguards into the design.

The ideal approach for driving LEDs is one in which the circuit monitors the current and keeps it constant. LEDs' forward voltage does not affect this type of circuit, eliminating the need for binning and the effect of the LEDs' negative forward-voltage-to-temperature coefficient. These circuits can be complex switching regulators or simple linear regulators with feedback loops. Complex switching regulators are ideal for high-light-output applications, such as streetlights.

Simple, economical, and robust hybrid circuits find use in architectural and interior-lighting fixtures. These circuits' design may be less efficient than that of a complex switching regulator, but their low cost and simplicity make them attractive. These circuits operate over the full universal voltage specifica-

### DI's Inside

42 Use op amps to make automatic-ORing power selector

45 Charging time indicates capacitor value

▶ See more Design Ideas at [www.edn.com/designideas](http://www.edn.com/designideas).

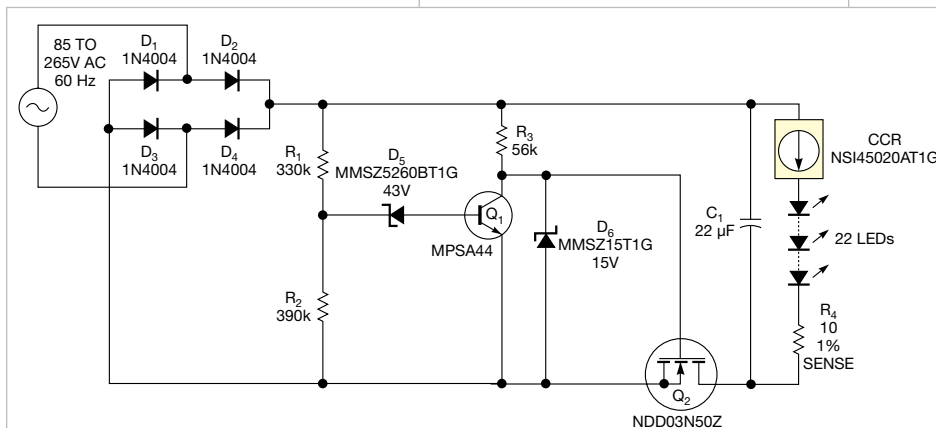
tion of 85 to 265V ac at 50 or 60 Hz.

The circuit in **Figure 1** comprises a bridge, a chopper, and a current regulator. The full-wave bridge comprising diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_4$ , feeds into the chopper circuit. MOSFET  $Q_2$  immediately turns on, and capacitor  $C_1$  begins to charge.

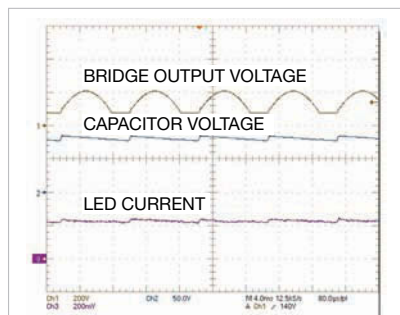
Resistors  $R_1$  and  $R_2$  form a voltage divider. When the voltage on the cathode of  $D_5$  reaches 43.5V, the zener diode conducts and turns on  $Q_1$ , which pulls the gate of  $Q_2$  low, causing it to turn off. Diode  $D_6$  protects  $Q_2$ 's gate.

The voltage across  $C_1$  stays at 80 to 90V. The charge on  $C_1$  feeds the CCR (constant-current regulator) and the LED string. This circuit example has 22 LEDs. The CCR maintains the current at 20 mA through the LED string. The circuit includes resistor  $R_4$  in series with the LEDs, for measuring the current through the LED string.

**Figure 2** shows the voltages at different parts of the cycle with an input voltage of 150V ac. Trace 1 is the output of the bridge-rectifier circuit. Trace 2 is the voltage across  $C_1$ , the output of the chopper circuit. Trace 3 is the voltage across the current-sense resistor. The traces clearly show that, when the voltage from



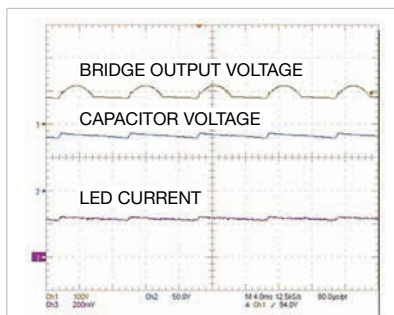
**Figure 1** This circuit drives a string of LEDs with a constant current over the entire worldwide range of ac-mains voltages.



**Figure 2** When the voltage from the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit.

the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit. **Figure 3** shows the voltages with an input voltage of 85V ac.

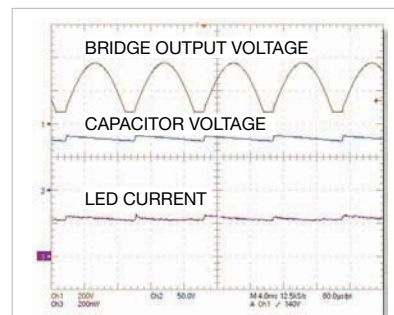
The oscilloscope traces show that there is still sufficient design head room, with  $Q_1$  staying on for a longer period,



**Figure 3** At 85V ac, the circuit continues to operate by keeping  $Q_1$  on for a longer period.

during which  $C_1$  fully charges. The input voltage drops to 54V ac before the current through the LEDs begins to drop.

**Figure 4** shows the circuit operation at an input voltage of 265V ac. Trace 1 shows that, because of its high input voltage,  $Q_1$  is on for a short time. Trace 2, however, shows that sufficient energy still remains to charge  $Q_1$  and maintain



**Figure 4** At 265V ac, the circuit has enough energy to keep  $C_1$  charged during off cycles.

the current through the LEDs during the off cycle.

You can scale this circuit to operate with different LED arrays. CCRs are available with current ratings as high as 160 mA. For higher currents, you can place the CCRs in parallel. The values of  $C_1$ ,  $R_1$ , and  $R_2$  match the type and number of LEDs. **EDN**

## Use op amps to make automatic-ORing power selector

Bob Zwicker, Analog Devices, Fort Collins, CO

Many systems must select among two or more low-voltage dc-input sources, such as an ac adapter, a USB (Universal Serial Bus) port, or an onboard battery, for example. You can implement this selection using manual switches, but automatic switching is preferable. You usually want to use the highest-available input voltage to power your system. You can accomplish this task using a Schottky-diode ORing scheme (**Figure 1**). Unfortunately, the forward-voltage drop of a Schottky diode ranges from 300 to 600 mV. This voltage wastes power, creates heat, and decreases the voltage available to your system.

Efficient voltage ORing requires only a P- or an N-channel MOSFET, a suitable op amp, and a few passives. This Design Idea describes the application of voltage ORing to positive dc-power rails. The P-channel-MOSFET design is suitable for low-power, single-supply

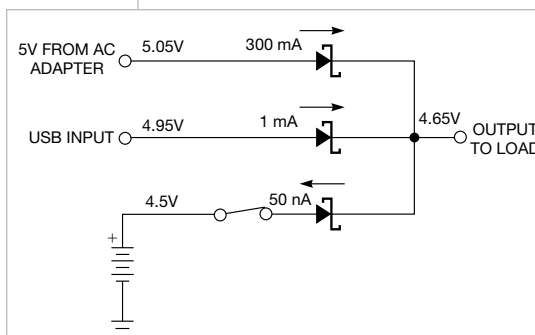
systems operating at 3.3V or higher, and the N-channel MOSFET fits situations in which the bus voltage is lower or the current is higher and a suitable op-amp bias voltage is available.

Positive current flows from the MOSFET drain in an N-channel-FET design. In a P-channel design, the current flows from the MOSFET source. The MOSFET's drain-body diode would defeat rectifier operation if the usual current flow (for switching or amplification) were used.

Your first design task is to choose a suitable MOSFET. The MOSFET's worst-case on-resistance must be low enough so that the  $I \times R$  (current-times-resistance) drop with full-load current is low enough to

accomplish the design objectives. A  $0.01\Omega$  MOSFET has a 50-mV forward-voltage drop when 5A flows through it. Be sure to consider power dissipation due to  $R \times I^2$  and the resulting temperature rise.

Your second design task is to choose an op amp. The op amp must be able to operate with the voltages involved and to adequately drive the MOSFET's gate voltage. The P-channel design requires a rail-to-rail I/O type. A single-supply op amp is adequate for the N-channel design. Another important consider-



**Figure 1** Schottky-diode ORing can power a load from the highest input-voltage source.

ation is the op amp's input offset voltage,  $V_{OS}$ . The total  $\pm V_{OS}$  window must be less than the maximum desired voltage drop across the MOSFET. For example, if you permit a 10-mV forward-voltage drop at full load, then the op amp should specify an offset voltage of  $\pm 5$  mV or better.

$R_1/R_2$ ,  $R_{11}/R_{12}$ , and  $R_{21}/R_{22}$  form the input-voltage divider, which biases the op-amp input at a level slightly below that of the input voltage that it is controlling (figures 2 and 3). This offset must exceed the op amp's maximum offset voltage to ensure that all op-amp parts in production always turn off the MOSFET when you apply reverse voltage. In the example of the P-channel 5V design,  $R_1$  and  $R_2$  bias the inverting op-amp input at 99.9% of the input voltage, or 4.995V dc. In steady-state

operation, the op amp servos with the conducting MOSFET to keep the other op amp's input at the same voltage, within the tolerance of the op amp's offset voltage. With a perfect 0V-offset op amp, light-load currents cause the MOSFET to only partially enhance, so the circuit delivers a 5-mV MOSFET forward-rectifier drop. This mild effect is the only disadvantage of  $R_1$  and  $R_2$ 's input offset biasing. If the MOSFET resistance is too high to allow it to maintain 5 mV at full load, then the op amp fully enhances the MOSFET as its output swings to the rail, and the ORing circuit delivers the MOSFET's fully enhanced on-resistance.

You can consider the MOSFET's variable on-resistance as the element with which the op amp senses current. When you apply reverse voltage, the

MOSFET de-enhances, the  $I \times R$  voltage drop increases, and the op amp's output ends up at the appropriate supply rail, driving off the MOSFET as hard as it can.

With light-load conditions and a given offset voltage, the op amp tries to servo the voltage on its power-output-sensing input to the voltage on its power-input-sensing input plus the offset voltage. With  $R_2$  open-circuited, the op amp has no intentional external offset. If the op amp's offset voltage were in the unfavorable direction, a sizable reverse-cutoff current would occur if the input-power bus were to fall to a lower potential than the output-voltage bus.

Figure 4 shows current-voltage test data for the operating region. The complete design, including intentional offset, produces the green curve. The

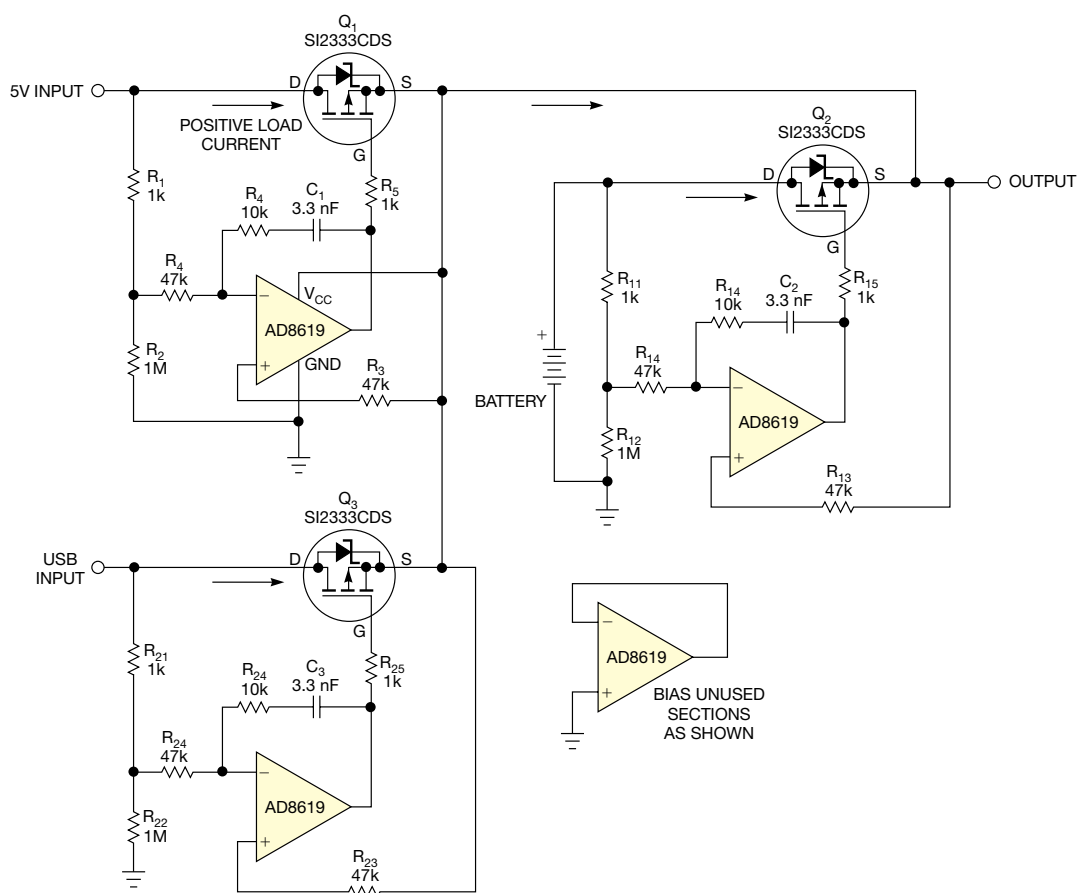


Figure 2 MOSFET power ORing using P-channel MOSFETs is the more common choice for single-rail systems when the rail voltage is sufficient to operate the op amp and drive the MOSFET gate.



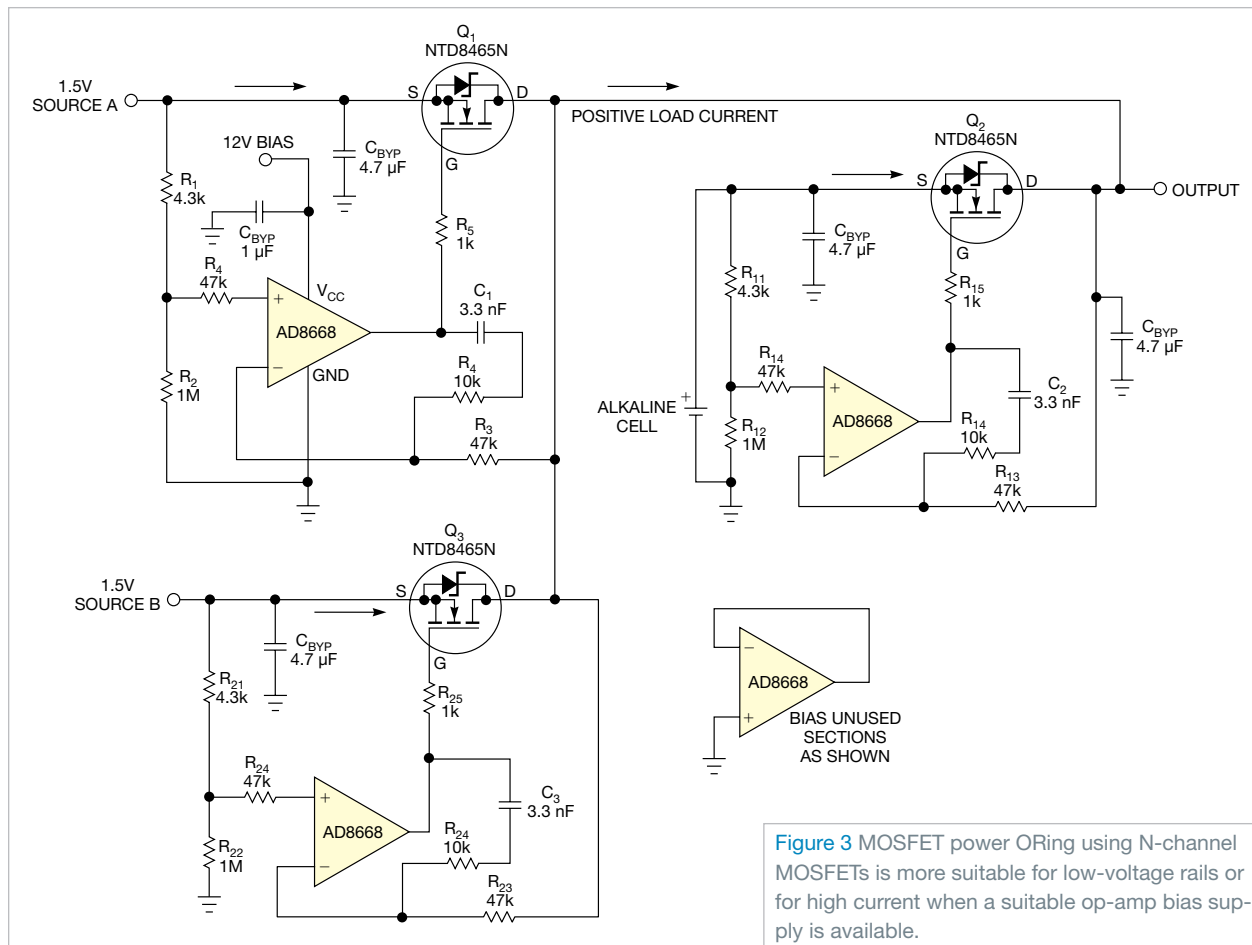


Figure 3 MOSFET power ORing using N-channel MOSFETs is more suitable for low-voltage rails or for high current when a suitable op-amp bias supply is available.

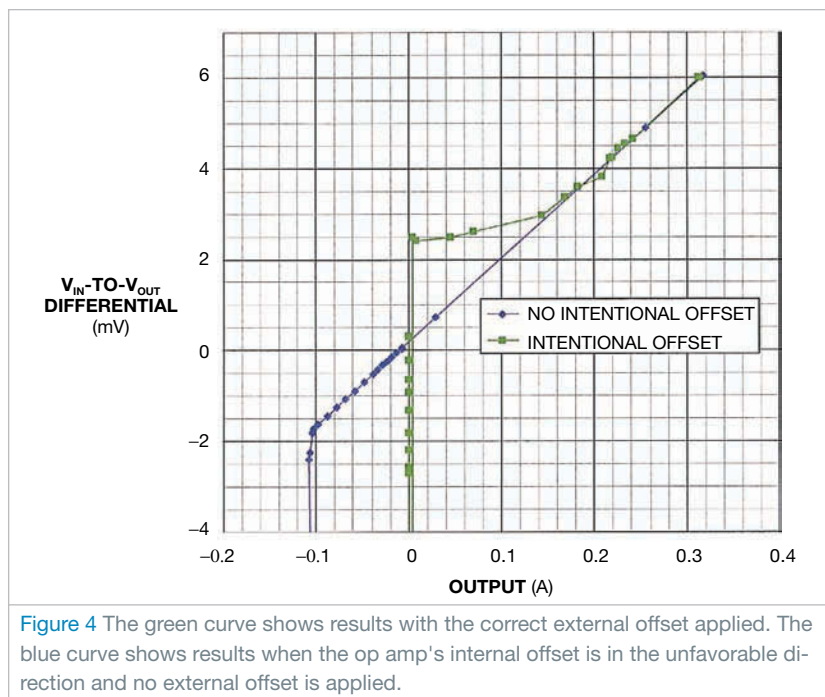


Figure 4 The green curve shows results with the correct external offset applied. The blue curve shows results when the op amp's internal offset is in the unfavorable direction and no external offset is applied.

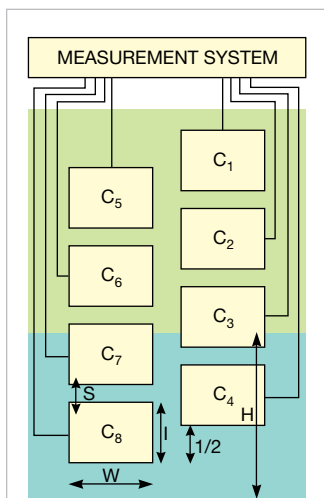
equivalent of an unfavorable internal offset and no intentional external offset produces the blue curve. Although the green curve sacrifices some forward-voltage drop at light-load conditions, its forward voltage is always less than the full-load maximum. The intentional offset avoids any significant reverse current in the MOSFET. This design can switch at the 0A current transition, at which the leakage-current MOSFET's drain-body diode is likely to dominate.

On the other hand, the blue curve, without intentional offset, permits significant reverse current under some circumstances. This example shows approximately 100-mA reverse current with 2-mV reverse voltage across the MOSFET before the circuit switches off the MOSFET. Both the P- and the N-channel designs have undergone testing, and the P-channel design is in production. **EDN**

# Charging time indicates capacitor value

Vlad Bande and Ioan Ciascai, Technical University of Cluj-Napoca, Cluj-Napoca, Romania

➔ A recent research project using a capacitive sensor to measure water levels comprises two PCB (printed-circuit-board) plates placed one in front of the other at a controlled distance. Every plate divides into eight equal copper zones, resulting in eight equivalent parallel-plate capacitors (**Figure 1**). Every capacitor has a plate area of 25 cm<sup>2</sup>. To measure the water's total height, the project uses a special hydro-insulated layer to avoid short circuits. Knowing the layer thickness and the electrical permittivity of the hydro-insulated substance allows you to express the distance between every two plates and the dielectric's electrical permittivity.



**Figure 1** Plates and a PCB's dielectric form a capacitor bank for measuring water level.

The capacitance of every two overlapped copper zones can vary only when the electrical permittivity changes because all other parameters—the plate's area and the distance between the plates—are constant, as the following **equation** shows:  $C_x = (\epsilon_0 \epsilon_r A) / D$ , where  $\epsilon_0 = (8.854 \times 10^{-12}) \text{ F/m}$ , the void electrical permittivity,  $\epsilon_r$  is the dielectric's relative electrical permittivity,  $D$  is the total dielectric thickness,  $C_x$  is the capacitance of the measured capacitor, and  $A$  is every plate's surface. The relative electrical

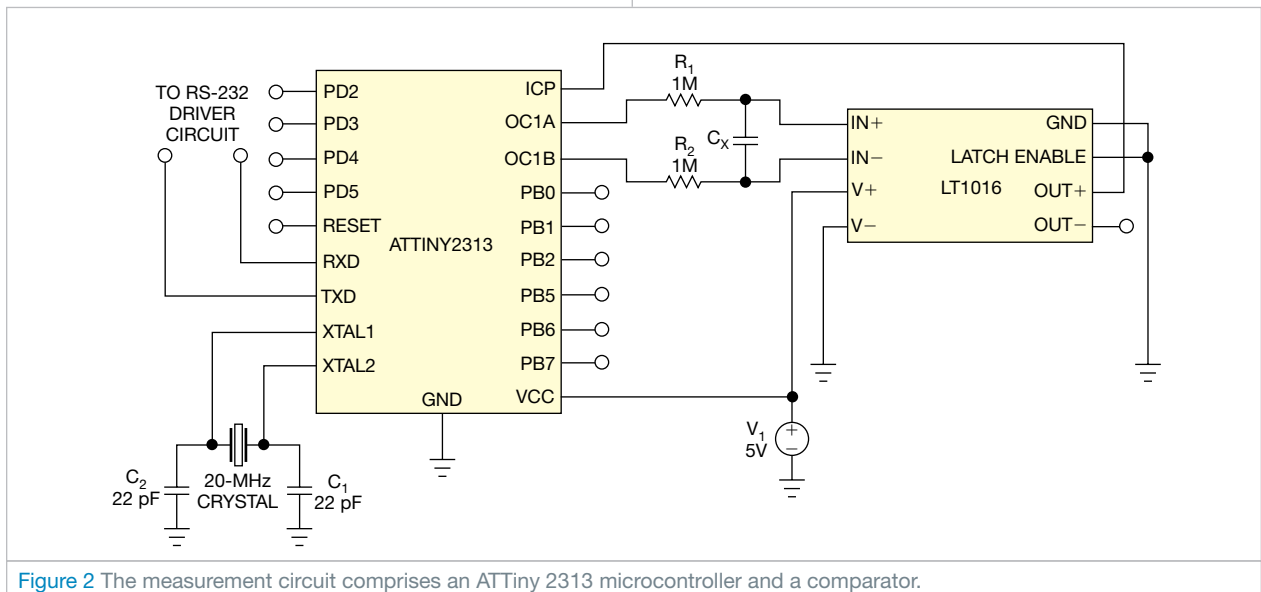
permittivity strictly depends on which and how many materials are between the capacitor plates. This application uses four kinds of  $\epsilon_r$ : air, air-hydro-insulated varnish, water-hydro-insulated varnish, and air-water-hydro-insulated varnish. At this point, you must consider the capacity of the capacitors at the surface-separation line between air and water.

To measure capacitance and thus measure the water level, a measurement system employs a 20-MHz ATtiny 2313 microcontroller and a fast LT1016 analog comparator (**Figure 2**). The measurement algorithm uses the microcontroller's OC1A and OC1B output-comparator signals. The ATtiny 2313 sets both pins at once but to opposite values. When OC1A is 5V, you can simultaneously set OC1B using assembly-language code. The same situation occurs when OC1B is 5V; OC1A is then 0V. In the first case, the quantity of the charge rises on the first plate and lowers on the other plate. Reversing the polarity causes the second plate to acquire more charge, and its potential rises. When both plates have the same potential, the LT1016 comparator enables the ICP pin on the microcontroller, saving the number in the internal timer counter and sending it through the serial port for further processing. When the voltages on both plates are equal, the voltage on the capacitor is halfway from the input signal's amplitude,  $V_{CC}/2$ .

The pulse width of both OC1A and OC1B must be larger than the maximum capacitor's charging time, which you obtain when you measure the water's dielectric capacitor, according to the following **equation**:  $PW \geq 10 \times R_e \times C_{MAX}$ . **Figure 3** shows the waveforms.

The charging **equation** in the transient region is:

$$\frac{V_{CC}}{2} = V_{CC} + [0 - V_{CC}] e^{-\frac{t}{2RC}} \Rightarrow \frac{1}{2} = e^{-\frac{N_1 t_{CLK}}{2RC}}$$



**Figure 2** The measurement circuit comprises an ATtiny 2313 microcontroller and a comparator.

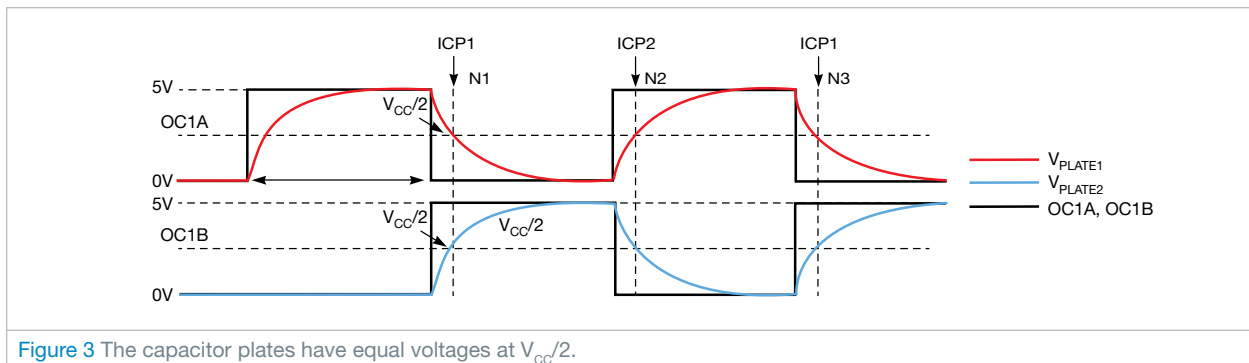


Figure 3 The capacitor plates have equal voltages at  $V_{CC}/2$ .

You can then extract the capacitance using the following equation:

$$C_x = \frac{N_1 t_{CLK}}{2R \ln 2},$$

or  $C_x = 0.036067376 \times N_1$  pF.

You can extract the level on both the left and the right side of the capacitive sensor in **Figure 1**, resulting in two equations but the same result. The algorithm consists of first measuring all the capacitors—completely immersed, partially immersed, and nonimmersed—and then express-

ing the surface of both  $C_7$ 's and  $C_3$ 's capacitor plates at the surface-separation line, using the unknown  $H$  variable. You then extract the unknown value of the level, obtaining both capacitive-dependent equations:

$$H = f\left(\frac{C_{PARTIALLYIMMERSED}}{C_{NONIMMERSED}}, L, \epsilon_{AIR}, \epsilon_{LAYER}, \epsilon_{WATER}, D_{AIR}, D_{LAYER}\right).$$

From the capacitive-measurement-procedure point of view, the designed system represents a floating measurement method that implies two similar parallel-plate armatures. This method halves the parasitic capacitances that occur during measurement referred to system ground. **EDN**

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# supplychain

LINKING DESIGN AND RESOURCES

## Apple still can't keep up with iPad demand

More than 15 months after the iPad was launched, Apple Inc (www.apple.com) still can't keep up with demand for the popular tablet. "This is a good problem; demand is fantastic," said Tim Cook (photo), Apple's chief operating officer, in a late-July conference call announcing record quarterly revenue and profits. It's still a problem, however, one that Apple would not talk about in detail. The company also alluded to a future product transition, which is one reason that it is forecasting a decline in sales for its fall quarter.

The good news is that Apple

when the company would be able to meet global demand. "We are working very hard to get as many units to customers as we can," he added.

Cook also dodged questions about whether the company planned to diversify its base of manufacturing partners beyond Foxconn, which operates city-sized factories for Apple in China. Supply-chain management is "part of our secret sauce, so I don't want to share too much about it," he explained. An explosion in May at a Foxconn plant in China may have affected iPad manufacturing (Reference 1).

Tablets are also cannibalizing notebook sales, but Cook



to continue to rise, but a future product transition may drag down sales and margins. Two-thirds of the margin decline will come from a different product mix in the fall quarter, said Peter Oppenheimer, Apple's chief financial officer. The rest of the decline, he added, would come from the future product transition and increased marketing expenses for the back-to-school quarter.

The product transition may come from the shift to iOS 5, which is due this fall. If the launch comes late in the quarter, it might slow iPhone and iPad sales until the company releases systems supporting it. Apple also faces a Mac transition with a new version of its operating system, Lion, which debuted last month. In addition, the company may need to refresh its iPod line, which continues to decline in sales by double digits. The newest member of the family, the iPod Touch, now makes up half the sales in the area.

Still on the distant horizon is a full-blown Web-connected TV product from Apple. To date the company has released two major versions of Apple TV, a

set-top box for streaming Web video, but no iTV product.

"Apple TV continues to do well, but we still call it a hobby here because we don't want anyone to think it's another leg of the stool like the iPhone," said Cook. "We continue to invest in it because we think there is something there."

The best news for Apple is that iPhone sales continue to grow, hitting 20.34 million units in the three months leading up to the call. Apple added 42 iPhone carriers in 15 countries in the last quarter, with much of the overall sales growth coming from emerging markets, such as Brazil, China, Mexico, and the Middle East.

Greater China, including Hong Kong and Taiwan, continues to expand rapidly as a market for Apple, growing six-fold to \$3.8 billion in sales in the current quarter compared with the same period last year. The region added \$8.8 billion to Apple's sales in the last three quarters, according to Cook.

Component supply also looks rosy to Apple. "Most components are in a positive supply situation, with prices falling at or above historical trends except hard-disk drives that are constrained and thus facing fewer price declines," Cook said.

—by Rick Merritt, *EE Times*  
This story was originally posted by EE Times: <http://bit.ly/oc8RXr>

### REFERENCE

1 Deffree, Suzanne, "Foxconn explosion ignites conversation on corporate responsibility," *EDN*, June 23, 2011, <http://bit.ly/oJ5y2v>.

 The good news is that Apple sold 9.25 million iPads in the last three months, double the number of the previous quarter.

sold 9.25 million iPads in the last three months, double the number of the previous quarter and three times as many as in the same quarter last year. The bad news is that it could have sold more if it had been able to manufacture them.

"In the first weeks of July, supply improved so that some SKUs [stock-keeping units] in some countries are now in supply/demand balance," said Cook, refusing to forecast

did not quantify the effect. "We believe some customers chose an iPad instead of a Mac but even more chose an iPad over a Windows PC, and there are more Windows PCs to cannibalize than Macs," he said.

Looking ahead, Apple predicts that its revenue will fall from \$28 billion this quarter to \$25 billion next quarter and that gross margins will slip from 41 to 38%. The company expects iPhone, iPad, and Mac sales

IMAGE: APPLE

# productroundup

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### IR's 40 to 75V automotive-qualified AU series MOSFETs deliver low on-resistance for heavy-load applications

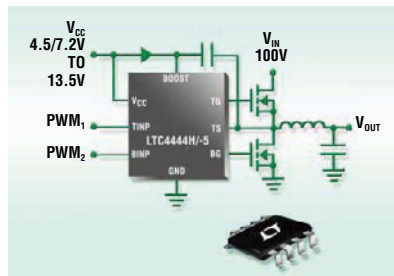
➔ The AU series of automotive-qualified MOSFETs are available in a variety of SMD and through-hole packages. One device in the series, the AU1RL1404S logic-level-gate-drive MOSFET, operates at 40V, and other devices in the series use standard-gate drives and operate at 40, 55, and 75V. The MOSFETs undergo dynamic- and static-part average testing and 100%-automated wafer-level visual inspection as part of the vendor's quality initiative targeting no defects. The vendor's BOM for the AU demonstrates a maximum on-resistance shift of less than 10% after 1000 temperature cycles of testing, exceeding AEC-Q101's qualification requiring no more than 20% change. Prices begin at 42 cents and \$1.22 (100,000) for the standard-gate-drive AU1RFZ44N and logic-level-gate-drive AU1RL1404S, respectively.

**International Rectifier, [www.irf.com](http://www.irf.com)**

### Linear Tech's LTC4444 and LTC4444-5 N-channel MOSFETs operate at -40 to +150°C

➔ The H-grade versions of the LTC4444 and LTC4444-5 gate drivers drive upper- and lower-power N-channel MOSFETs in synchronous-rectified-converter topologies. The devices operate over a junction temperature of -40 to +150°C, compared with the I-grade version's -40 to +125°C operating-temperature range. The devices integrate shoot-through protection to minimize dead time and prevent both the upper and the lower MOSFETs from con-

ducting simultaneously. The drivers can source as much as 1.4A with a 1.5Ω pull-

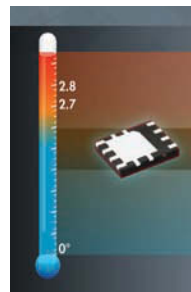


down impedance for driving the top MOSFET and a source current of 1.75A with a 0.75Ω pulldown impedance for the bottom MOSFET, making it ideal for driving high-gate-capacitance, high-current MOSFETs. The devices can drive multiple MOSFETs in parallel for higher-current applications. The upper MOSFET has an 8-nsec rise time and a 5-nsec fall time, and the lower MOSFET has 6- and 3-nsec rise and fall times, respectively, minimizing switching losses. The devices have supply-independent inputs and internally level-shift the high-side input logic signal to the bootstrap supply, which can function as much as 114V above ground. The LTC4444-5 drives both upper and lower MOSFETs over a range of 4.5 to 13.5V, and the LTC4444 drives both upper and lower MOSFET gates over a range of 7.2 to 13V. Both parts are available in a thermally enhanced MSOP-8 package, and prices start at \$2 (1000).

**Linear Technology Corp, [www.linear.com](http://www.linear.com)**

### Fairchild's 60V PowerTrench MOSFET touts low conduction and switching losses


➔ The 60V FDMS86500L N-channel PowerTrench MOSFET provides 2.5-mΩ on-resistance at a gate-to-source voltage of 10V and a drain current of 25A, enabling lower conduction losses in an industry-standard 5×6-mm Power 56 package. The FDMS86500L uses shielded-gate-MOSFET technology, providing a typical gate-to-drain charge of 14.6 nC. The device offers a better on-resistance-times-gate-to-drain-charge figure of merit, delivering high efficiency and lower power dissipation to meet efficiency stan-



dards and regulations. The FDMS86500L sells for 90 cents (1000).

**Fairchild Semiconductor,**  
www.fairchildsemi.com

## Vishay's 45V TMBS rectifiers target photovoltaic-solar-cell bypass protection

 The TMBS (trench-MOS-barrier-Schottky) series of rectifiers includes 12 45V devices in three power packages that feature a 10 to 60A current range. Typical forward voltage decreases to 0.33V at 10A, making the rectifiers



applicable in solar-cell junction boxes as bypass diodes for protection. The dual-chip VT1045CBP, VT2045CBP, VT3045CBP, and VT6045CBP come in power TO-220AB, ITO-220AB, and TO-263AB packages. All rectifiers feature a maximum operating junction tem-

perature of 150°C and a maximum junction temperature of 200°C or less in dc forward current without reverse bias for one hour or less. Prices start at 60 cents (one to 9999).

**Vishay Intertechnology Inc,**  
www.vishay.com

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## On the dark side



In the early 1980s, I was working on a specialized computer-terminal CRT display for a flight-management computer my company was designing for a major aircraft company. The display had to be bright enough to see in the cockpit in direct sunlight and also had to be dimmable for nighttime flight. The display used stroke-written characters to get the needed brightness and dissipated minimal power.

To optimize the stroke-written character set for the application, we initially selected a 2716 UV (ultraviolet) EPROM, which would enable us to experiment and quickly make changes. One of the engineers worked on the character set and programmed a 2716 for the characters we needed. We tested it, and everything worked fine. We soon realized, however, that the recently introduced 2732 EPROM would probably obsolete the 2716. It was still early in the design cycle, so we decided to use the 2732 instead. It came in the same package and had the same pinout as the 2716 except for an extra address bit, so it was an easy change. We programmed a 2732 and inserted it in the socket on the breadboard. Everything worked fine.

We continued testing other aspects of the design, working out other bugs here and there.

It was getting closer to a major design review. Our customer would be visiting and expected to see the prototype in operation. We were confident that the demo would go flawlessly because we had tested the heck out of it. What could go wrong? For the demonstration, we wanted to show the customer that an operator could dim the display to low light for nighttime operation. Although we had measured the light output and confirmed that it was in spec, the numbers on the test instrumentation were less impressive than a demo would show. We asked facilities to build us a “darkroom” in the lab so that we could demonstrate

the display in both bright-sunlight and dark conditions.

We then moved all the breadboards and test equipment into the room. A short time later, one of the engineers came into my office and told me about a problem. Whenever he turned off the lights, the display went dark after 10 seconds. When he turned on the lights, the display lit up again.

After some thought, we realized that the original schematic wired up only the address lines that the 2716 used and that we had forgotten to wire the extra address line of the 2732. Yet the 2732 had been running fine in the lab for months. We then realized that the lab always had light coming through the quartz window that allowed the UV EPROM to be erased. We had never bothered to cover the window because we were still in development mode, and the light in the lab was too dim to erase the UV EPROM in any reasonable time. The extra address line on the 2732 happened to go to a low logic level in the light but drifted to a high logic level in the dark. That action would select the half of the EPROM that we had not programmed, which also happened to be the program for all space characters. Therefore, the entire display went blank.

Now that we knew the root cause of the problem, we could easily fix it. The major design review with our customer was a success. The demo worked flawlessly both in bright light and in total darkness.

The next day, one of the engineers called me into the darkroom and informed me of a new problem. When he turned off the light, the entire display changed to Chinese characters. When he flipped the switch back on, everything returned to English. I realized that, in a celebratory mood after our successful demo, he was pulling a prank on me. He had programmed half of the 2732 with Chinese characters and wired up the floating address line with a switch to either let the address line float or connect it to ground. We both laughed and went back to work. **EDN**

**Walter Sjursen is the chief technology officer at Songbird Hearing Inc (North Brunswick, NJ).**

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